Bt856

Bt857

YCrCb or RGB to NTSC/PAL Digital Video Encoder

The Bt856/7 is designed specifically for video systems requiring the generation of 525-line (NTSC/PAL–M) or 625-line (PAL–B, D, G, H, I, N, N-Argentina) composite or Y/C (S-video) signals.

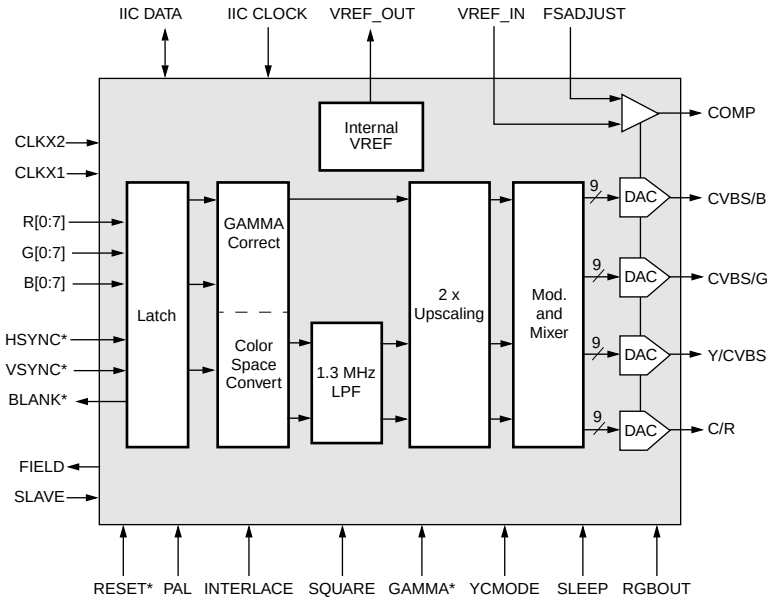
The Bt856 and Bt857 are functionally identical, with the exception that Bt857 can output the Macrovision anticopy algorithm.

Horizontal sync (HSYNC*) and vertical sync (VSYNC*) may be configured as inputs (slave mode) or outputs (master mode). BLANK* is an input and may be externally controlled.

24-bit linear or gamma-corrected RGB data or 4:2:2 YCrCb data may be input. The rise and fall times of sync, the burst envelope, and closed caption data are internally controlled.

Analog luminance (Y) and chrominance (C) information is available on the Y and C outputs for interfacing to S-video equipment. The composite analog video signal is output simultaneously onto two analog outputs. This allows one output to provide baseband composite video and another output to drive an RF modulator. Analog RGB is available to support the European SCART/PeriTV interface.

Functional Block Diagram



Distinguishing Features

- RGB or YCrCb Inputs, Selectable on a Pixel-by-Pixel Basis
- NTSC/PAL/PAL–M/PAL–N (Argentina) Composite Video Output
- S-Video/RGB Outputs Supported
- CCIR 601 or Square Pixel Operation
- 2x Oversampling
- 9-bit DACs
- Master or Slave Video Timing
- Noninterlaced Operation
- Macrovision Support (Bt857 Only)
- Closed Captioning Encoding
- Power-Down Mode
- SCART Support (RGB Outputs)
- I^2C Interface
- On-Board Voltage Reference
- Internal Color Bar Generator
- 68-pin PLCC Package

Related Products

- Bt819
- Bt851
- Bt856EVM

Applications

- Digital Set Top Box
- Direct Broadcast Satellite (DBS)
- Digital Video Disk (DVD)
- Digital VCR
- VideoCD

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Ordering Information

Model Number	Package	Ambient Temperature Range
Bt856KPJ	68-Pin Plastic J-Lead	0˚ to +70˚C
Bt857KPJ	68-Pin Plastic J-Lead	0˚ to +70˚C

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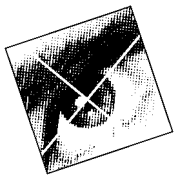
TABLE OF CONTENTS

List of Figures

List of Tables



CIRCUIT DESCRIPTION

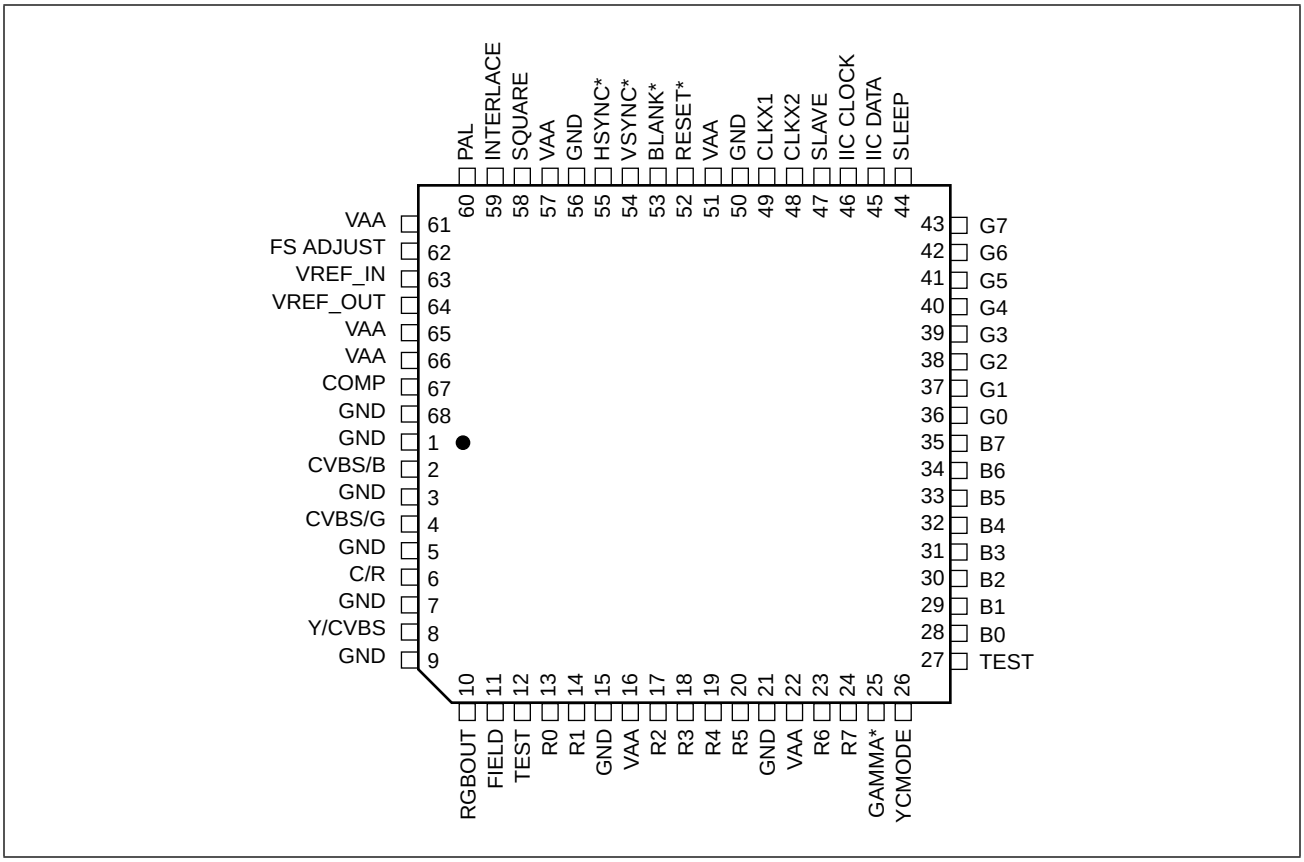
Pin Descriptions

Pin Name	I/O	Pin #	Description
CVBS/B	O	2	Composite video with blanking and sync, or Blue.
CVBS/G	O	4	Composite video with blanking and sync, or Green.
C/R	O	6	Modulated chrominance, or Red.
Y/CVBS	O	8	Luminance (with blanking, sync, and, optionally, Macrovision pulses, and/or closed-captioning encoding), or Composite video.
RGBOUT	I	10	Analog RGB control input (TTL compatible). A logical one configures the device to output analog RGB (RGBOUT mode). A logical zero configures the device to generate S-video along with a second composite video output. This pin may be connected directly to VAA or GND.
FIELD	O	11	Field control output (TTL compatible). FIELD transitions after the rising edge of CLOCK, two clock cycles following falling HSYNC*. It is a logical zero during odd fields and is a logical one during even fields.
TEST	I	12, 27	These pins are reserved for testing and must be connected to a logical zero, such as GND, for normal operation.
GAMMA*	I	25	RGB gamma control input (TTL compatible). In RGB mode, a logical zero enables the gamma correction circuitry. For RGB mode, a logical one provides a linear response. In 8-bit YC mode, this pin is used to select between inputs on B0–B7 (logical one) or G0–G7 (logical zero) pixel ports. In RGBOUT mode, if bit D4 of register 0xDC is low, this pin can be used to enable upsampling (logical zero) or disable upsampling (logical one). In RGBOUT mode, the GAMMA* pin will also select an oversampling filter (on the G0–G7 port for 8-bit YCmode) when low, unless overridden by the combination of bits D2 at subaddress 0xDA and D4 at subaddress 0xDC. This override will enable/disable oversampling for any input to RGB outputs. This pin may be connected directly to VAA or GND.
YC MODE	I	26	RGB or YCrCb select input (TTL compatible). A logical one configures the pixel inputs for YCrCb operation (YC mode). A logical zero configures the pixel inputs for RGB operation (RGB mode), and can be switched on each clock cycle. This pin may be connected directly to VAA or GND.

Pin Name	I/O	Pin #	Description
SLEEP	I	44	Powerdown control input (TTL compatible). A logical one configures the device for power-down mode. A logical zero configures the device for normal operation. This pin may be connected directly to VAA or GND.
IIC DATA	I/O	45	Serial interface data input/output (TTL compatible). Data is written to and read from the device via this serial bus.
IIC CLOCK	I	46	Serial interface clock input (TTL compatible). The maximum clock rate is 100 kHz.
SLAVE	I	47	Slave/master mode select input (TTL compatible). A logical one configures the device for slave video timing operation. A logical zero configures the device for master video timing operation. This pin may be connected directly to VAA or GND. This pin is ignored if bit D4 of subaddress register 0xDC is a logical one.
CLKX2	I	48	2x pixel clock input (TTL compatible).
CLKX1	I	49	Pixel clock input (TTL compatible). Inverted and Sampled by CLKX2 to derive CLOCK.
RESET*	I	52	Reset control input (TTL compatible). A logical zero for one CLOCK cycle resets and disables video timing (horizontal, vertical, subcarrier counters to the start of VSYNC of first field). A logical zero for two CLOCK cycles also resets internal registers to 00. RESET* must be a logical one for normal operation, commencing at the start of VSYNC.
BLANK*	I	53	Composite blanking control input (TTL compatible). BLANK* is registered on the rising edge of CLOCK. The R0–R7, G0–G7, and B0–B7 inputs are ignored while BLANK* is a logical zero.
VSYNC*	I/O	54	Vertical sync input/output (TTL compatible). As an output (master mode operation), VSYNC* is output following the rising edge of CLOCK. As an input (slave mode operation), VSYNC* is registered on the rising edge of CLOCK.
HSYNC*	I/O	55	Horizontal sync input/output (TTL compatible). As an output (master mode operation), HSYNC* is output following the rising edge of CLOCK. As an input (slave mode operation), HSYNC* is registered on the rising edge of CLOCK.
SQUARE	I	58	Square pixel/CCIR 601 resolution select input (TTL compatible). A logical one configures the device for square pixel operation. A logical zero configures the devices for CCIR 601 resolution operation. This pin should be connected directly to GND if using I^2C. This pin is ignored if bit D4 of subaddress register 0xDC is a logical one, or if PAL M or N-Argentina is selected via bits D0, D1 of register 0xDA.
INTERLACE	I	59	Interlaced/noninterlaced mode select input (TTL compatible). A logical one configures the device for interlaced operation. A logical zero configures the device for noninterlaced operation. This pin should be connected directly to GND if using I^2C. This pin is ignored if bit D4 of subaddress register 0xDC is a logical one.

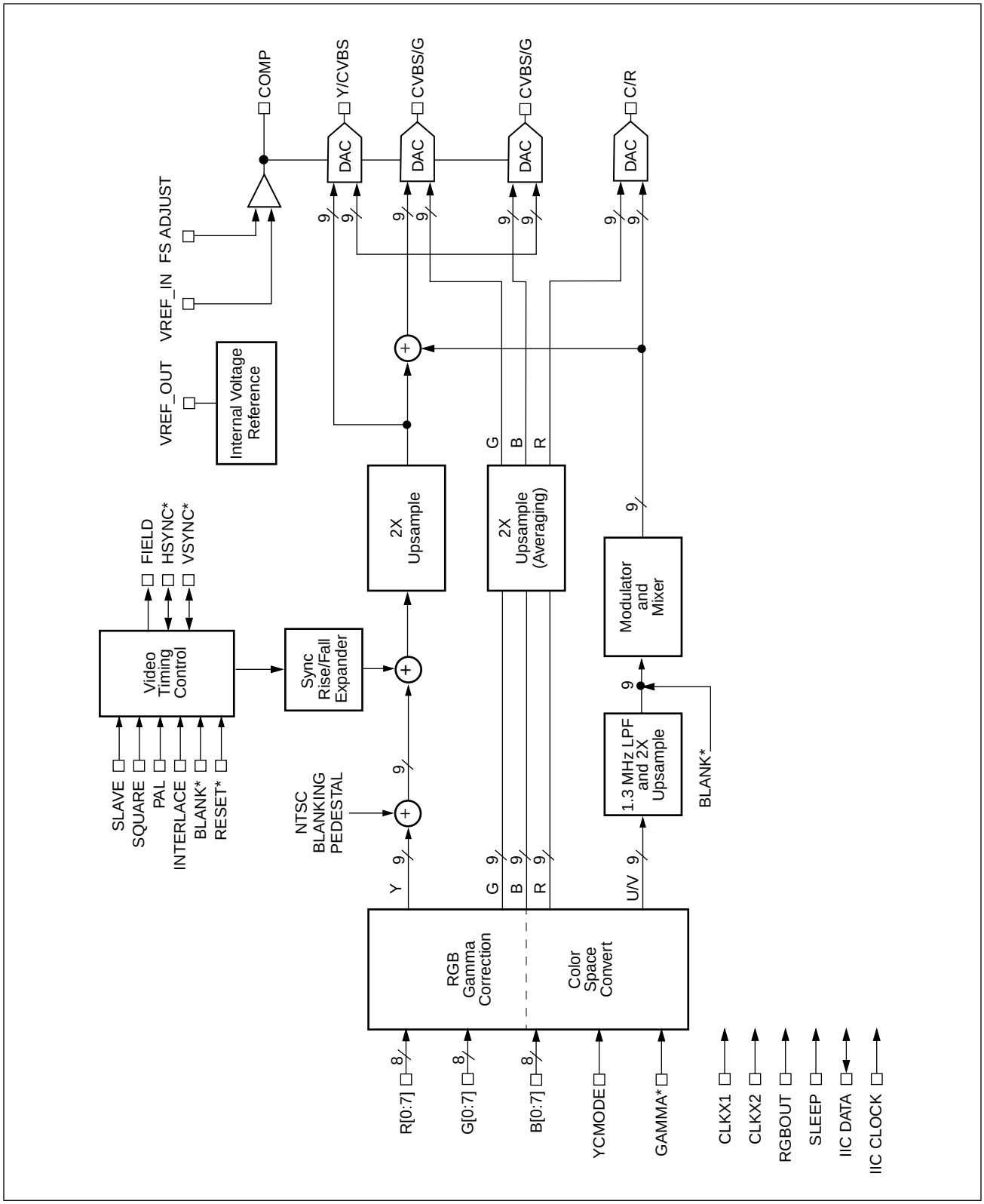
Pin Name	I/O	Pin #	Description
PAL	I	60	NTSC/PAL mode select input (TTL compatible). A logical one configures the device for PAL (B, D, G, H, I, N) operation. A logical zero configures the device for NTSC operation. This pin should be connected directly to GND if using I^2C. For non-I^2C use, a 10 kΩ pullup resistor (to VAA) MUST be used to program the Bt856/7 for PAL operation. Since this pin is also used as an analog test pin, it cannot be connected directly to VAA or VDD. This pin is ignored if bit D4 of subaddress register 0xDC is a logical one. To enable PAL–M or PAL–N (Argentina), bits D1 and D0 of register 0xDA and D5 of register 0xDC (for PAL-M setup) must be set.
FS ADJUST		62	Full-scale adjust control pin. A resistor (RSET) connected between this pin and GND controls the full-scale output current on the analog outputs. For standard operation, use the nominal RSET values shown under Recommended Operating Conditions. The relationship between RSET and the full-scale output current on the DAC outputs is: RSET (Ω) = 2,055 * VREF_IN (V) / Iout FS (mA)
VREF_IN	I	63	Voltage reference input. VREF_IN may be connected directly to VREF_OUT. An external voltage reference can supply this input with a 1.235 V (typical) reference. A 0.1 µF ceramic capacitor must be used to decouple this input to GND, as shown in Figures 15 and 16 in the PC Board Layout section. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF_OUT	O	64	Voltage reference output. This pin should only be used to drive the VREF_IN pin. See Figure 16.
COMP		67	Compensation pin. A 0.1 µF ceramic capacitor must be used to bypass this pin to VAA. The capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
R0–R7, G0–G7, B0–B7	I	13,14, 17–20, 23,24 36–43, 28–35	RGB or YCrCb (G7:B0) pixel inputs (TTL compatible). A higher index corresponds to a greater significance.
VAA	–	16,22, 51,57, 61,65, 66	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
GND	–	15,21,50,56 68 1,3,5,7,9	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.

Figure 1. Bt856/7 Pinout Diagram



A detailed block diagram of the Bt856/7 is shown in Figure 2.

Figure 2. Detailed Block Diagram



Clock Timing

Both CLKX1 and CLKX2 must be supplied to Bt856/7. The internal CLOCK is derived by registering inverted CLKX1 with the rising edge of CLKX2. Synchronous inputs and outputs are registered by the rising edge of CLOCK, except in 8-bit YCrCb input mode where Cb/Cr are registered on the falling edge of CLOCK. The timing parameters specified under AC Characteristics in the Parametric Information section are defined with respect to CLKX2. Inputs must be valid for the minimum specified setup time prior to the rising edge of CLKX2 while CLKX1 is low (except in 8-bit YCrCb mode where Cb/Cr are registered while CLKX1 is high).

Pixel Input Timing

24-bit RGB Input Mode

R0–R7, G0–G7, B0–B7 are registered on the rising edge of CLOCK. This mode is enabled by setting the YCMODE pin low.

16-bit YCrCb Input Mode

This mode is available by setting the YCMODE pin high. Y0–Y7 data is input via the G0–G7 inputs; multiplexed Cb0–Cb7 and Cr0–Cr7 data is input via the B0–B7 inputs. G0–G7 and B0–B7 are registered on the rising edge of CLOCK. R0–R7 and GAMMA* pins are ignored.

8-bit YCrCb Input Mode

The 8-bit YCrCb multiplexed input mode is selected by setting the YCMODE pin high and by setting register bit D7 of register 0xDC to a 1. Multiplexed Y, Cb, and Cr data is input through the G0–G7 inputs or through the B0–B7 inputs. The GAMMA* pin is used to select between the two different 8-bit ports: if GAMMA* is high, YCrCb is input through B0–B7; if GAMMA* is low, YCrCb is input through G0–G7. By default, the input sequence for active video pixels must be Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3, etc. in accordance with CCIR656.

Y and Cb/Cr are registered during a single CLOCK period. Cb or Cr is registered first, on the falling edge of CLOCK; Y is registered next, on the rising edge of CLOCK.

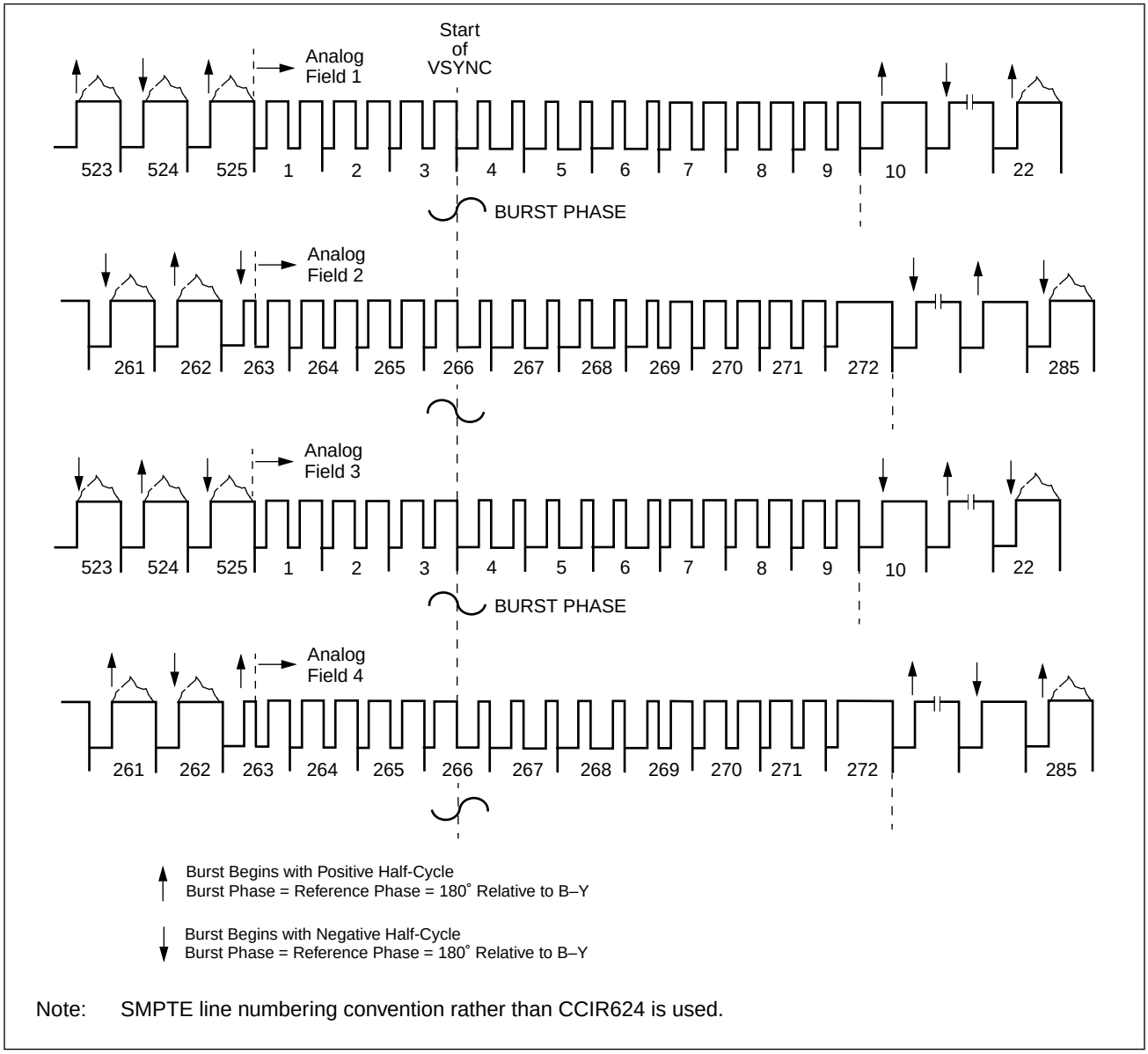
CBFLAG Timing

By default, Cb data is input during odd (base1) values of the horizontal counter while Cr data is registered during even counts. Cb data may be input during even values of the horizontal counter by writing a 1 to register bit D6 of register 0xDC. The falling edge of HSYNC* corresponds to a horizontal count of one (default after RESET* cycle) unless the Bt856/7 is configured in master mode with programmable HSYNC* output timing.

Video Timing

The width of the analog horizontal sync pulses and the start and end of color burst is automatically calculated and inserted for each mode according to CCIR624-4. Color burst is disabled on appropriate scan lines. Serration and equalization pulses are generated on appropriate scan lines. In addition, rise and fall times of sync, closed-caption data transitions, and the burst envelope are internally controlled. Figures 3–6 show the timing characteristics for various Bt856/7 modes of operation.

Figure 3. Interlaced 525-Line (NTSC, PAL-M) Video Timing



Note: SMPTE line numbering convention rather than CCIR624 is used.

Figure 4a. Interlaced 625-Line (PAL–B, D, G, H, I, N, N-Argentina) Video Timing

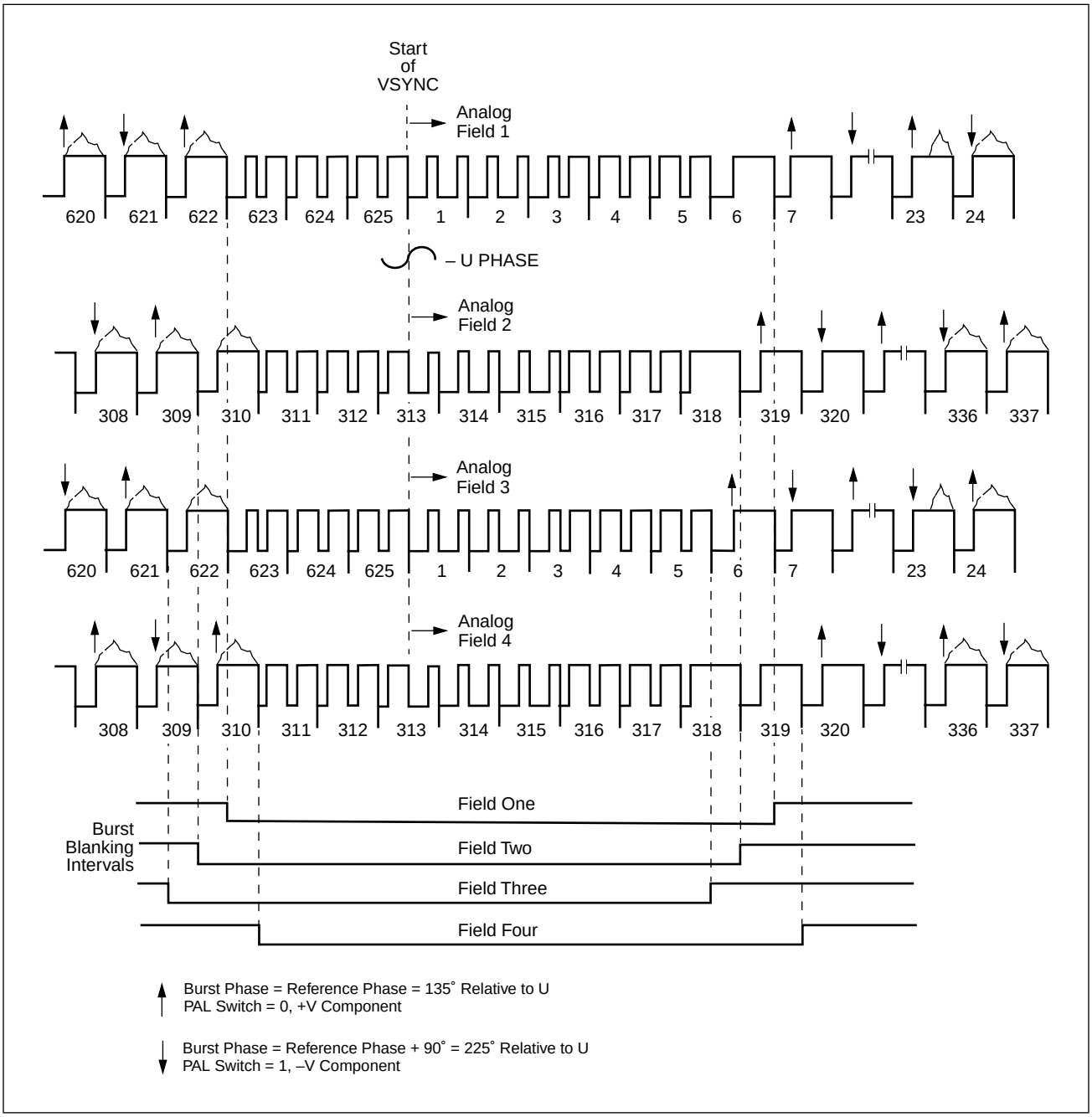


Figure 4b. Interlaced 625-Line (PAL–B, D, G, H, I, N, N-Argentina) Video Timing

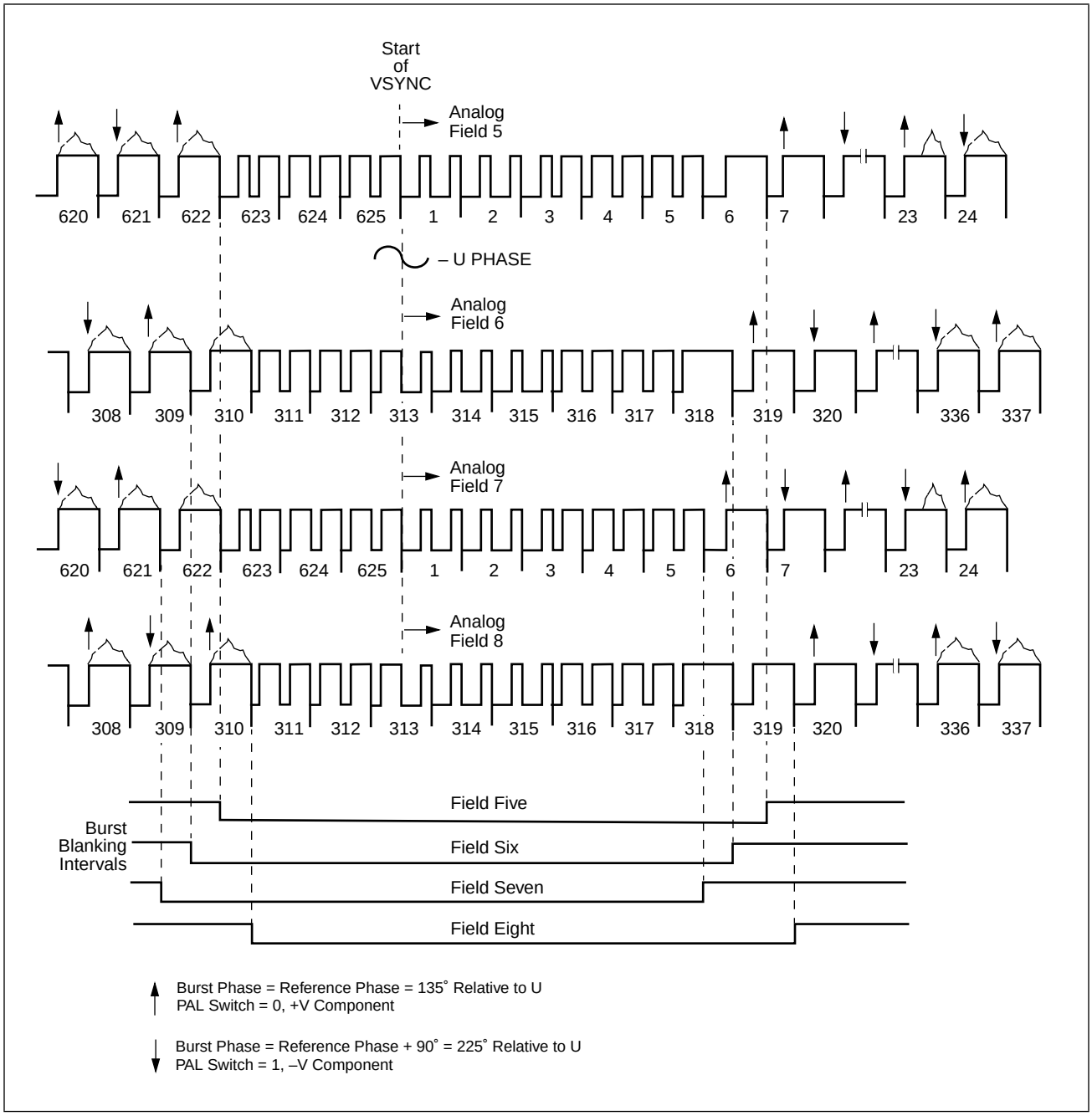


Figure 5. Noninterlaced 262-Line (NTSC, PAL-M) Video Timing

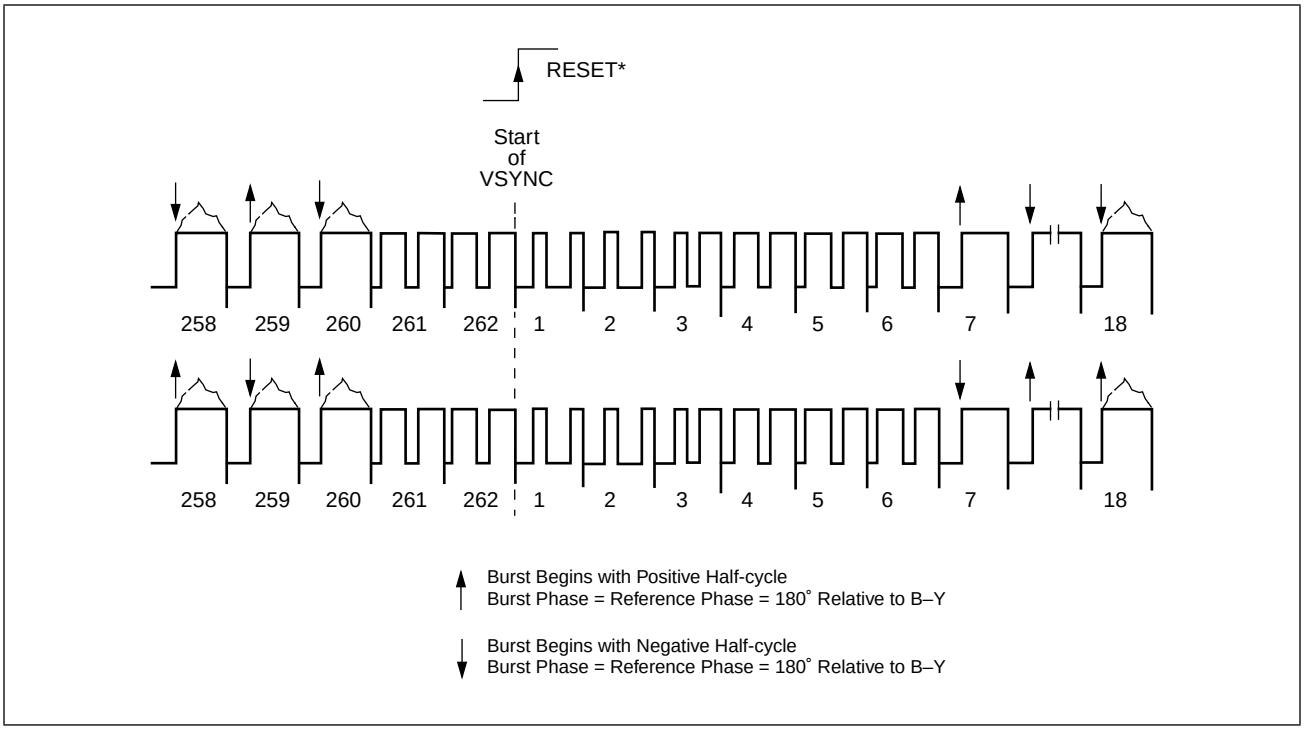
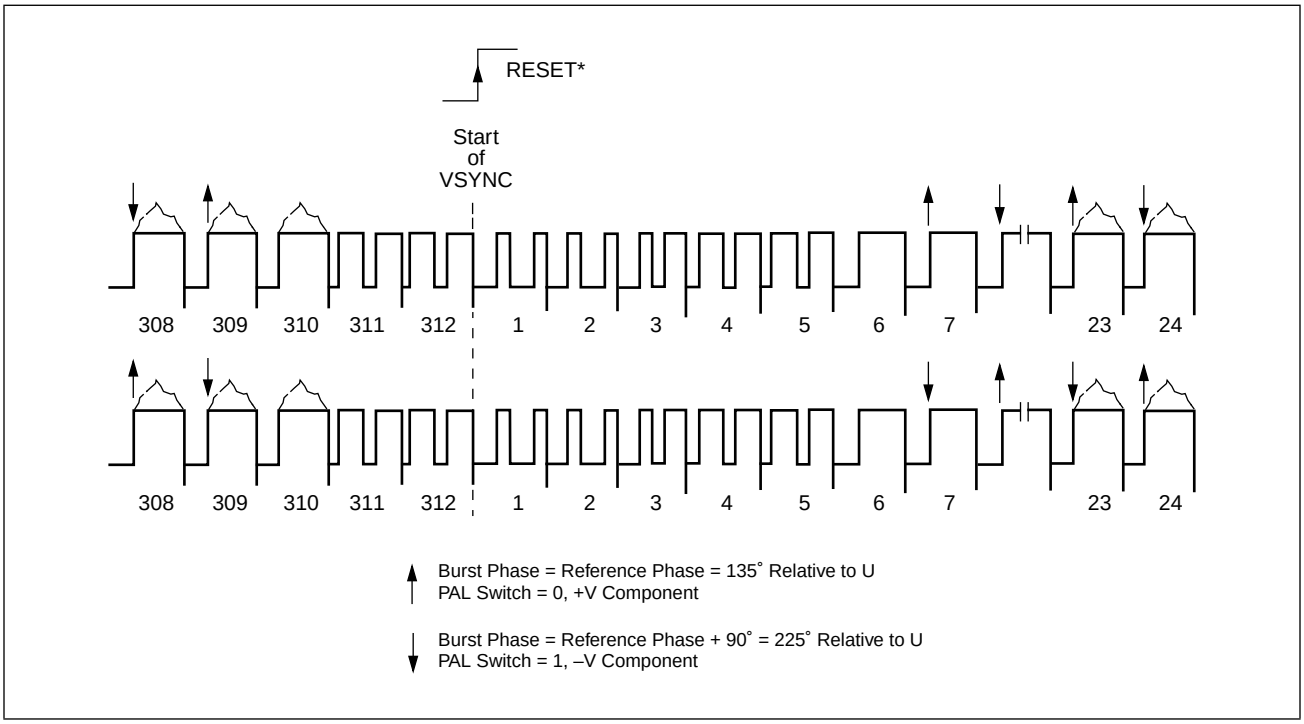


Figure 6. Noninterlaced 312-Line (PAL–B, D, G, H, I, N, N-Argentina) Video Timing



Reset

If the RESET* pin is held low during a single rising edge of the internally generated CLOCK signal, the subcarrier phase is set to zero, and the horizontal and vertical counters are set to the beginning of VSYNC of FIELD1. Counting resumes the first rising edge of CLOCK after rising RESET*.

In addition to the timing reset, if the RESET* pin is held low for two consecutive low-to-high transitions of CLOCK, a software reset occurs, setting all of the software programmable registers' bits to zero.

Master Mode

Horizontal sync (HSYNC*) and vertical sync (VSYNC*) are generated from internal timing and from optional software bits. HSYNC* and VSYNC* are output following the rising edge of CLOCK.

The horizontal counter is incremented on the rising edge of CLOCK. After reaching the appropriate value (determined by the mode of operation), it is reset to one, indicating the start of a new line.

The vertical counter is incremented at the start of each new line. After reaching the appropriate value (determined by the mode of operation), it is reset to one, indicating the start of a new field (interlaced operation) or frame (noninterlaced operation).

The HSYNC* output may be configured to have standard video timing (4.7 µs wide, asserted at start of a line default after RESET cycle) or it may be programmed to specify the start of HSYNC* (10-bit value) and the end of HSYNC* (10-bit value). VSYNC* is asserted for 3 or 2.5 scan lines for 262/525 line and 312/625 line, respectively. When HSYNC* is configured for standard video timing, coincident falling edges of HSYNC* and VSYNC* indicate the beginning of an odd field.

Slave Mode

Horizontal sync (HSYNC*) and vertical sync (VSYNC*) are inputs that are registered on the rising edge of CLOCK.

The horizontal counter is incremented on the rising edge of CLOCK. A falling edge of HSYNC* resets it to one, indicating the start of a new line.

The vertical counter is incremented on the falling edge of HSYNC*. A falling edge of VSYNC* resets it to one, indicating the start of a new field (interlaced operation) or frame (noninterlaced operation).

A falling edge of VSYNC* that occurs within ±1/4 of a scan line from the falling edge of HSYNC* indicates the beginning of an odd field. A falling edge of VSYNC* that occurs within ±1/4 scan line from the center of the line indicates the beginning of an even field. Referring to Figures 3–6, start of VSYNC occurs on the falling HSYNC* at the beginning of the next expected odd field and halfway between expected falling HSYNC* edges at the beginning of the next expected even field.

The operating mode is automatically determined when configured as a slave. The PAL, INTERLACE, and SQUARE pins are ignored. The mode override registers can still be used to force a particular mode. 525-line operation is assumed; 625-line operation is detected by the number of lines in a field. Interlaced operation is detected by observing the sequence of odd or even fields; if the field timing (odd follows odd, even follows even) is repeated, then noninterlaced mode is as-

sumed. The frequency of operation (square pixels or CCIR) for both PAL and NTSC is detected by counting the number of clocks per line. The sampling note is assumed to be 13.5 MHz unless the exact horizontal count for square pixels, ±1 count, is detected in between two successive falling edges of HSYNC*.

NOTE: Square pixel 625-line operation with this sequence requires one frame to stabilize.

FIELD Output

The FIELD output indicates whether an odd field (logical zero) or even field (logical one) is being generated. Field changes are detected by the falling edge of VSYNC*. FIELD is output following the rising edge of CLOCK. Unless special HSYNC* timing is programmed, FIELD output transitions low, two CLOCK periods following the falling edge of HSYNC* at the beginning of an odd field.

This corresponds directly to the bottom/top* convention of some MPEG decoders.

Pixel Blanking

BLANK* is registered on the rising edge of CLOCK. For RGBOUT mode, RGB video is blanked for each clock period in which the BLANK* input is low. For video outputs, BLANK* is pipelined to match the luminance and chrominance paths and is applied to the digital video before analog conversion. The automatic horizontal blanking sequence described in Table 10 (in the PC Board Considerations section) take precedence over the BLANK* input.

Burst Blanking

For interlaced NTSC/PAL–M, color burst information is automatically disabled on scan lines 1–6 and 264–269, inclusive. (SMPTE line numbering convention.)

For interlaced PAL–B, D, G, H, I, N, N-Argentina, color burst information is automatically disabled on scan lines 1–6, 310–318, and 623–625, inclusive, for fields 1, 2, 5, and 6. During fields 3, 4, 7, and 8, color burst information is disabled on scan lines 1–5, 311–319, and 622–625, inclusive.

For noninterlaced NTSC/PAL–M, color burst information is automatically disabled on scan lines 1–6 and 261–262, inclusive.

For noninterlaced PAL–B, D, G, H, I, N, N-Argentina, color burst information is automatically disabled on scan lines 1–6 and 310–312, inclusive. See Figures 3–6.

Digital Processing

Once the input data is converted into internal YUV format, the UV components are low-pass filtered with a filter response shown in Figure 7 (linearly scalable by clock frequency). The Y and filtered UV components are upsampled to CLKX2 frequency by a digital filter whose response is shown in Figure 8.

Chrominance Disable

The chrominance subcarrier may be turned off by setting bit D5 of register subaddress 0xDE to a logical one. This kills burst as well, providing luminance only signals on the CVBS outputs and a static blank level on the C/R output (RGBOUT=0).

Figure 7. Three-Stage Chroma Filter

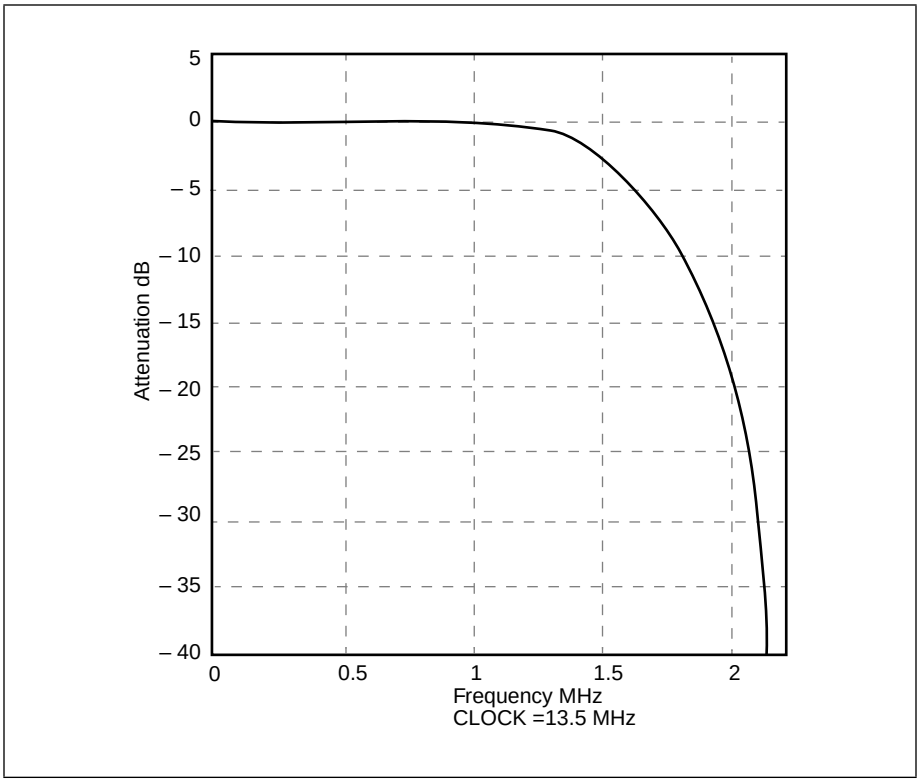
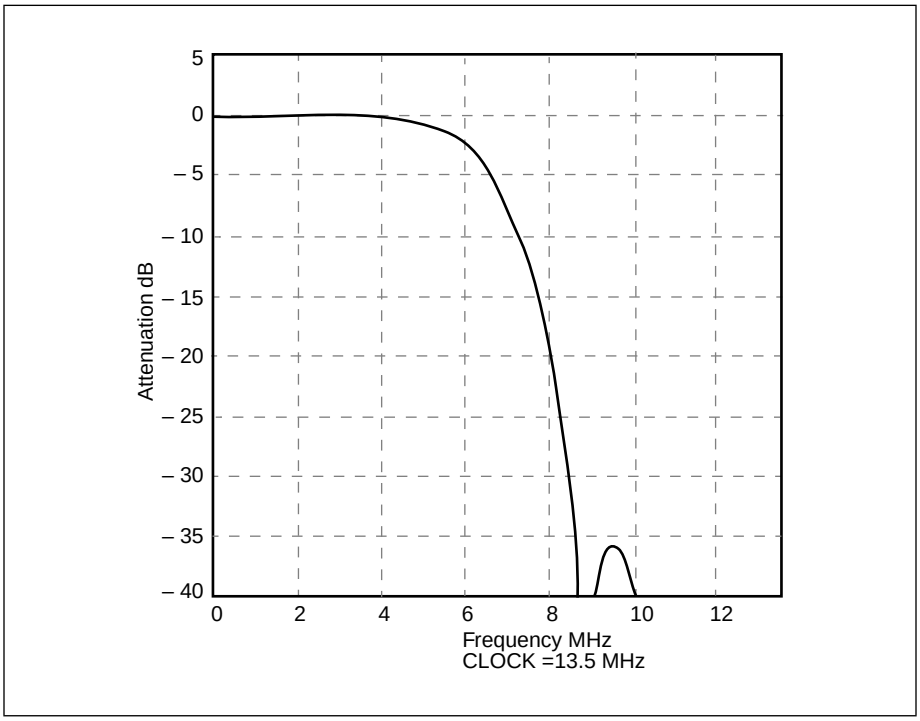


Figure 8. Luminance Upsampling Filter Response



Subcarrier Phasing

In order to maintain correct SC-H phasings, subcarrier phase is set to zero on the falling edge of HSYNC* associated with VSYNC* every four (NTSC) or eight (PAL) fields, unless bit D3 of register 0xDE is set to a logical one.

In slave mode, falling HSYNC* may lag falling VSYNC* by 1/4 scan line but cannot precede falling VSYNC* by more than 14 CLOCK periods for correct SC-H reset.

Setting D3 to one may be useful in situations where the ratio of CLOCKS/HSYNC* edges in a color frame is non-integer, which could produce a significant phase impulse by resetting to zero.

For a perfect clock input, the burst frequency is 4.43361875 MHz for PAL–B, D, G, H, I, N, 3.57561149 for PAL–M, 3.58205625 for PAL–N (Argentina), 3.579545 MHz for NTSC interlaced, and 3.579515 MHz for NTSC noninterlaced.

Vertical Blanking Intervals

For interlaced NTSC/PAL–M, scan lines 1–9 and 263–272, inclusive, are always blanked regardless of the BLANK* input. There is no setup on scan lines 10–21 and 273–284, inclusive, allowing the generation of video test signals, timecode, and other information by controlling the pixel inputs appropriately (except for lines controlled by closed caption or Macrovision generation).

For interlaced PAL–B, D, G, H, I, N, N-Argentina, scan lines 1–6, 311–318, and 624–625, inclusive, during fields 1, 2, 5, and 6, are always blanked regardless of the BLANK* input. During fields 3, 4, 7, and 8, scan lines 1–5, 311–319, and 624–625, inclusive, are always blanked regardless of the BLANK* input. The remaining scan lines during the vertical blanking interval may be used for the generation of video test signals, timecode, and other information by controlling the pixel inputs appropriately.

Alternately, all displayed lines in the vertical blanking interval (10–21 and 273–284 for interlaced NTSC/PAL–M; 7–13 and 320–335 for interlaced PAL–B, D, G, H, I, N, N-Argentina) may be forced blanked by setting bit D2 to a logical one in register 0xDE (except for caption lines controlled by bit D6 and D7 or Macrovision process).

For noninterlaced NTSC/PAL–M, scan lines 1–9, inclusive, are always blanked regardless of the BLANK* input. For noninterlaced PAL–B, D, G, H, I, N, N-Argentina, scan lines 1–6 and 311–312, inclusive, are always blanked regardless of the BLANK* input.

Bit D2 at register 0xDE will blank lines 10–21 for NTSC/PAL–M or lines 7–23 for PAL–B, D, G, H, I, N, N-Argentina, except for closed captions on lines 21 (22) and 284 (335), controlled by bits D6 and D7, or for Macrovision process.

Noninterlaced Operation

The device can be operated in noninterlaced mode by setting the INTERLACE pin to a logical zero. When in noninterlaced master mode, the Bt856/7 always displays the odd-field, meaning that the falling edges of HSYNC* and VSYNC* will be output coincidentally. FIELD will change state with each VSYNC* edge. Additionally, a 30 Hz offset will be subtracted from the color subcarrier frequency while in NTSC/PAL–M mode so that the color subcarrier phase will be inverted from field to field. Subcarrier phase is reset to zero upon rising RESET* and every 4 fields of NTSC/PAL–M or 8 fields of PAL–B, D, G, H, I, N, N-Argentina, unless bit D3 in register 0xDE is a logical one.

Transition from interlaced to noninterlaced in master mode, occurs during odd fields to prevent synchronization disturbance. In slave mode, transition occurs after a subsequent falling edge of VSYNC*.

NOTE: Consumer VCRs can record noninterlaced video with minor noise artifacts, but special effects (e.g., scan > 2x) may not function properly.

Power-Down Mode

In power-down mode (SLEEP pin set to 1), register states are preserved, but other chip functionality (including I^2C communication) is disabled.

This mode should be set when the Bt856/7 may be subjected to clock and data frequencies outside its functional range.

Pixel Input Ranges and Colorspace Conversion

RGB Inputs

With YCMODE set to a logical zero (RGB mode), digital RGB data with a 0–255 range is input via the R0–R7, G0–G7, and B0–B7 inputs. By default, the gray-scale range of 0–255 represents 7.5–100 IRE for NTSC, or 300–1000 mV for PAL.

Alternatively, software bit D5 of register 0xDC can alter pixel scaling and disable or enable the 7.5 IRE setup. When this bit is enabled, PAL video can be generated using NTSC/PAL–M blanking levels and 7.5 IRE setup, and default NTSC/PAL–M pixel scaling is applied (0–255 represents 7.5–100 IRE); or, NTSC/PAL–M video can be generated using PAL scaling (0–255 represents 0–100 IRE) without the 7.5 IRE setup. NTSC mode with setup disabled has 2% less black-to-white range compared to setup enabled.

If the GAMMA* pin is high, no prescaling is performed to compensate for gamma characteristics of the receiver. If GAMMA* is low, gamma pre-correction is applied per CCIR 709. In the following equations, *x* represents the pixel input value and *g* represents the corrected value.

525-Line Systems (NTSC, PAL–M):

$$\text{for } x < 5,\ g = 4.5 * x$$
$$\text{for } x > 4,\ g = 255 * (1.099 * (x/255)(1/2.2) - 0.099)$$

625-Line Systems (PAL–B, D, G, H, I, N, N–Argentina):

$$\text{for } x < 5,\ g = 9 * x$$
$$\text{for } x > 4,\ g = 255 * (1.099 * (x/255)(1/2.8) - 0.099)$$

The standard CCIR 624 matrix is used to convert RGB to YUV:

$$Y = +0.299R + 0.587G + 0.114B$$
$$U = -0.147R - 0.289G + 0.436B$$
$$V = +0.615R - 0.515G - 0.100B$$

NTSC 33% axis rotation is performed in the subcarrier encoding. Data is rounded to the nearest 9-bit DAC value.

For RGBOUT mode (RGBOUT = 1 with YC mode = 0), the 8-bit RGB inputs directly feed the 9-bit DACs without any scaling or level-shifting. Therefore, only half of the current drive is available in this mode. Gamma precorrection is not applied to RGB outputs.

An averaging interpolation filter is available to upsample the RGB pixel stream. Upsampling is enabled or disabled in either of two ways: with the GAMMA* pin or with software bit D2 of register 0xDA. The pin-override switch (bit D4 of register 0xDC) determines which method has priority: if the override is high, then software is used; if the override is low, then the GAMMA* pin is used. In both cases (GAMMA* pin or bit D2 of register 0xDA), a logical low enables upsampling and a logical high disables upsampling. The pipeline delay is the same regardless of whether upsampling is active or not (please see AC Characteristics for pipeline delay).

YC Inputs (4:2:2 YCrCb)

Y has a nominal range of 16–235; Cb and Cr have a nominal range of 16–240, with 128 equal to zero. Values of 0 and 255 are interpreted as 1 and 254, respectively. Y values of 1–15 and 236–254, and CrCb values of 1–15 and 241–254, are interpreted as valid linear values.

Alternatively, software bit D5 of register 0xDC can alter pixel scaling and disable or enable the 7.5 IRE setup. When this bit is enabled, PAL–B, D, G, H, I, N, N-Argentina video can be generated using NTSC/PAL–M blanking levels and 7.5 IRE setup, and NTSC/PAL–M pixel scaling is performed (Y range of 16-235 represents 7.5-100 IRE); or, NTSC/PAL–M video can be generated using PAL–B, D, G, H, I, N, N-Argentina scaling (Y range of 16-235 represents 0-100 IRE) without the 7.5 IRE setup. NTSC/PAL–M mode with setup disabled has 2% less black-to-white range than NTSC/PAL–M mode with setup enabled.

For RGBOUT mode, 4:2:2 YCrCb digital component video will be used to generate composite video and will be converted to the RGB colorspace to drive the RGB DACs. The Y input range of 16–235 will produce a range of 0.7 V at the output. Since YC values outside of the nominal range are allowed, the black level is raised above zero volts to allow for Y values less than 16, and the output range of the DACs can exceed 0.7 V to allow for Y values above 235. The conversion is linearly scaled in the overshoot and undershoot regions. The following matrix, based on CCIR 601, is used to convert YCrCb to RGB:

$$R = Y + 1.371*Cr$$
$$G = Y - 0.699*Cr - 0.337*Cb$$
$$B = Y + 1.733*Cb$$

Values are rounded to 9-bits at the DAC.

An averaging interpolation filter is available to upsample the RGB pixel stream. Upsampling is enabled or disabled in either of two ways: with the GAMMA* pin or with software bit D2 of register 0xDA. The pin-override switch (bit D4 of register 0xDC) determines which method has priority: if the override is high, then software is used; if the override is low, then the GAMMA* pin is used. In both cases (GAMMA* pin or bit D2 of register 0xDA), a logical low enables upsampling and a logical high disables upsampling. The pipeline delay is the same regardless of whether upsampling is active or not (please see AC Characteristics for pipeline delay).

DAC Coding

White is represented by a DAC code of 400. For PAL–B, D, G, H, I, N, N-Argentina, the standard blanking level is represented by a DAC code of 120. For NTSC/PAL–M, with setup enabled (bit D5 of register 0xDC is ‘0’), the standard blanking level is represented by a DAC code of 114, 1 IRE is equivalent to a DAC code of 2.857. For NTSC/PAL–M with setup disabled (bit D5 of register 0xDC is ‘1’), the standard blanking level is represented by a DAC code of 112, 1 IRE is equivalent to a DAC code of 2.800.

Closed Captioning

The Bt856/7 encodes NTSC/PAL–M closed captioning on scan line 21 and NTSC/PAL–M extended data services on scan line 284. Four 8-bit registers (subaddress 0xD0–D4) provide the data while bits D6 and D7 at subaddress 0xDE enable display of the data. A logical zero corresponds to the blanking level of 0 IRE, while a logical one corresponds to 50 IRE above the blanking level.

Closed captioning for PAL–B, D, G, H, I, N, N-Argentina is similar to that for NTSC. Closed caption encoding is performed for 625-line systems according to the system proposed by the National Captioning Institute; clock and data timing is identical to that of NTSC system, except that encoding is provided on lines 22 and 335.

The Bt856/7 generates the clock run-in and appropriate timing automatically. Pixel inputs are ignored during CC encoding. See FCC Code of Federal Regulations (CFR) 47 Section 15.119 (10/91 edition or later) for programming information. EIA608 describes ancillary data applications for Field 2 Line 21 (line 284).

NOTE: Register contents are transferred immediately following the clock run-in, and must be stable for the duration of the line generated.

Anticopy Process (Bt857 Only)

The anticopy process contained within the Bt857 is implemented according to the Macrovision revision 6 specification developed by Macrovision in Mountain View, California. All luminance, chrominance, and composite video waveforms include the Macrovision anticopy process. The Bt857 incorporates an anticopy process technology that is protected by U.S. patents and other intellectual property rights. The anticopy process is licensed for non-commercial, home use only. Reverse engineering or disassembly is prohibited.

Brooktree cannot ship Bt857 units to any customer until that customer has been approved by Macrovision. To obtain approval for shipment of Bt857 samples, a “Macrovision Proprietary Material License Agreement” is required. Contact Macrovision at 415-691-2900 (FAX: 415-691-2999) to facilitate this agreement.

Internal Color Bars

The Bt856/7 can be configured to generate 75% amplitude, 100% saturation (75/7.5/75/7.5 for NTSC/PAL–M with setup; 75/0/75/0 for PAL) color bars, regardless of the GAMMA* pin state.

If the IIC DATA pin is held high during the rising edge of RESET*, color bars are automatically enabled. Otherwise, following a reset, colorbars can be enabled or disabled by writing a one or a zero into bit D4 of register 0xDE. With the exception of the YCMODE and GAMMA* pins, all pins and registers can be changed and reprogrammed while generating color bars, thereby simplifying testing of various modes.

If the IIC DATA pin is held low while the RESET* pin goes high, color bars will not be generated following a reset condition. The IIC DATA pin is normally high, unless performing a data transfer or acknowledge pulse.

SCART/PeriTV Support

The RGBOUT pin may be used to configure the Bt856/7 to generate analog RGB video signals (rather than S-video) to interface to a SCART/PeriTV connector. When RGBOUT = 1, red information is output on the C/R pin, blue information is output on the CVBS/B pin, and green information is output on the CVBS/G pin. Composite video will be present on the Y/CVBS DAC, but will not be time-aligned with RGB outputs. In RGB mode, nominal RGB amplitude is 635 mVpp with a 37.5 Ω load, while in YC mode, RGB outputs are 700 mVpp into 37.5 ohms.

Software Programming

A simplified I^2C (7-bit subaddress, 100 Kbps) interface is provided for programming the registers. All registers are write-only and are set to zero following a software reset. All data transfers and addresses are written MSB first. The LSB for all subaddresses is zero to indicate a write condition.

Registers can be written if the I^2C address 0x88 is received. The device ID can be read from the IIC DATA pin if the address 0x89 is received. The device ID for the Bt857 is 0xE0; for the Bt856, it is 0x60. Figure 17 in the PC Board Considerations section illustrates I^2C write operations.

CLKX2 and CLKX1 must be applied and stable for IIC communication. Activating SLEEP or RESET* will disable IIC communication. Following power up, the IIC DATA pin may be asserted until CLOCK cycles four times.

Outputs

All digital-to-analog converters are designed to drive standard video levels into an equivalent 37.5 Ω load. Unused outputs should be connected directly to ground to minimize supply switching currents. In standard mode (RGBOUT = 0), two composite video and S-Video (YC) outputs are available. In RGBOUT mode (RGBOUT = 1), one composite video output along with Analog RGB are available (see Table 1). If the SLEEP pin is high, the DACs are essentially turned off and only the leakage current is present. The D/A converter values for 100% saturation, 100% amplitude color bars are shown in Figures 9–14. Both composite video and analog RGB video (to provide support for SCART/PeriTV) may be generated simultaneously.

Table 1. DAC Output Cross-Reference

Pin Name	Pin Number	Pin Function	
		Std Mode	RGB Out Mode
CVBS/B	2	CVBS	B
CVBS/G	4	CVBS	G
C/R	6	C	R
Y/CVBS	8	Y	CVBS

Luminance or CVBS (Y/CVBS) Analog Output

Digital luminance information drives the 9-bit D/A converter that generates the analog Y video output (Figures 9 and 10 and Tables 2 and 3). This DAC can also provide CVBS for SCART/PeriTV synchronization when RGBOUT is enabled.

Chrominance or Red (C/R) Analog Output

Digital chrominance information drives the 9-bit D/A converter that generates the analog C video output (Figures 11 and 12 and Tables 4 and 5). This DAC can also provide Red for SCART/PeriTV when RGBOUT is enabled.

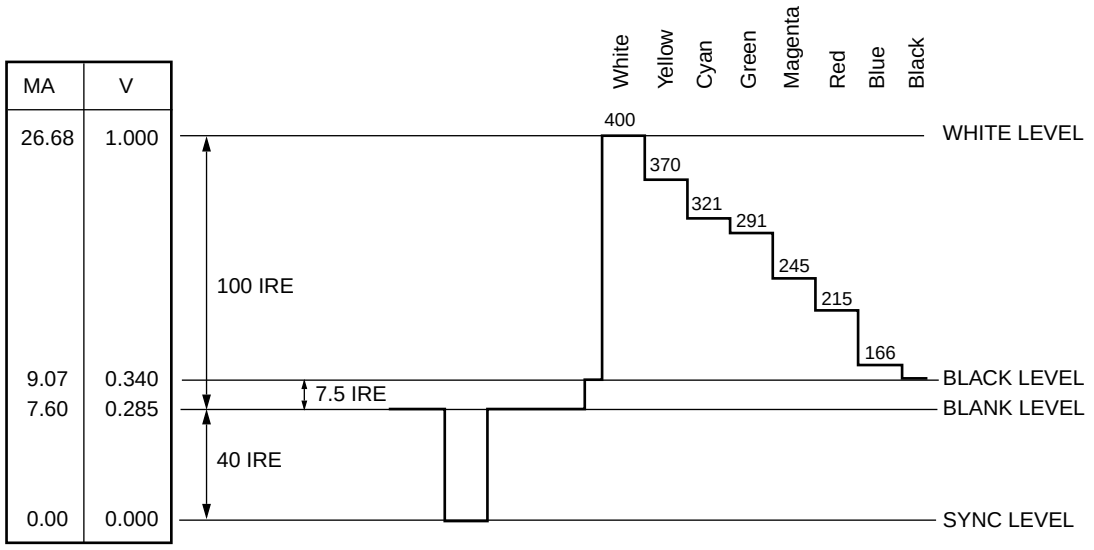
Composite Video or Blue (CVBS/B) Output

Digital composite video information drives the 9-bit D/A converter that generates the analog NTSC or PAL video output (Figures 13 and 14 and Tables 6 and 7). This DAC can also provide Blue for SCART/PeriTV when RGBOUT is enabled.

Composite Video (CVBS/G) Analog Output

Digital composite video information drives the 9-bit D/A converter that generates the analog video output (Table 8). This DAC can also provide Green for SCART/PeriTV when RGBOUT is enabled.

Figure 9. 525-Line (NTSC/PAL–M) Y (Luminance) Video Output Waveform



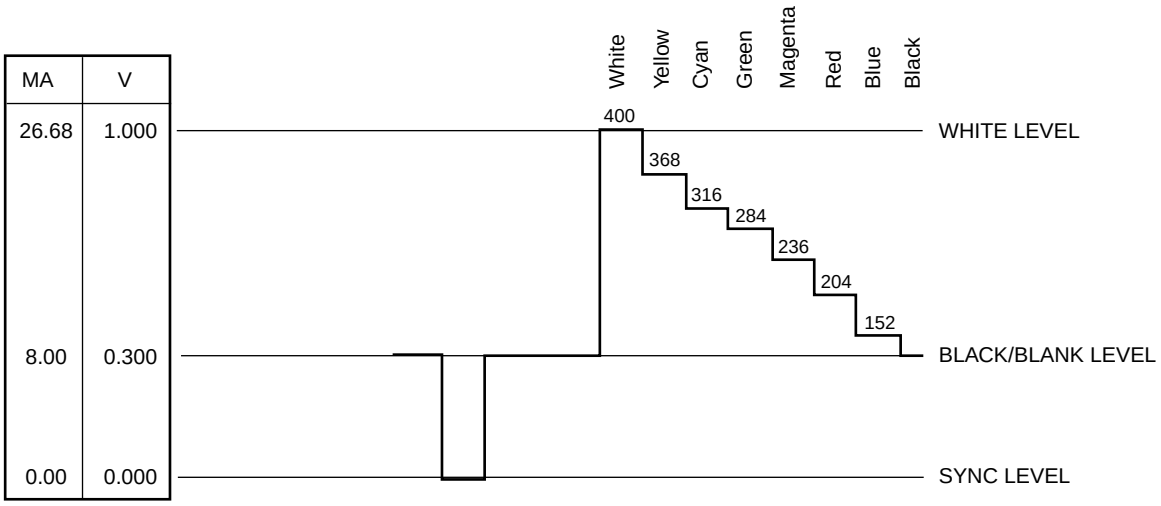
Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, Nominal RSET, and setup on. SMPTE 170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Table 2. 525-Line (NTSC/PAL–M) Y (Luminance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*
White	26.68	400	0	1
Black	9.07	136	0	1
Blank	7.60	114	0	0
Sync	0	0	1	0

Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, Nominal RSET, and setup on. SMPTE 170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Figure 10. 625-Line (PAL–B, D, G, H, I, N, N-Argentina) Y (Luminance) Video Output Waveform



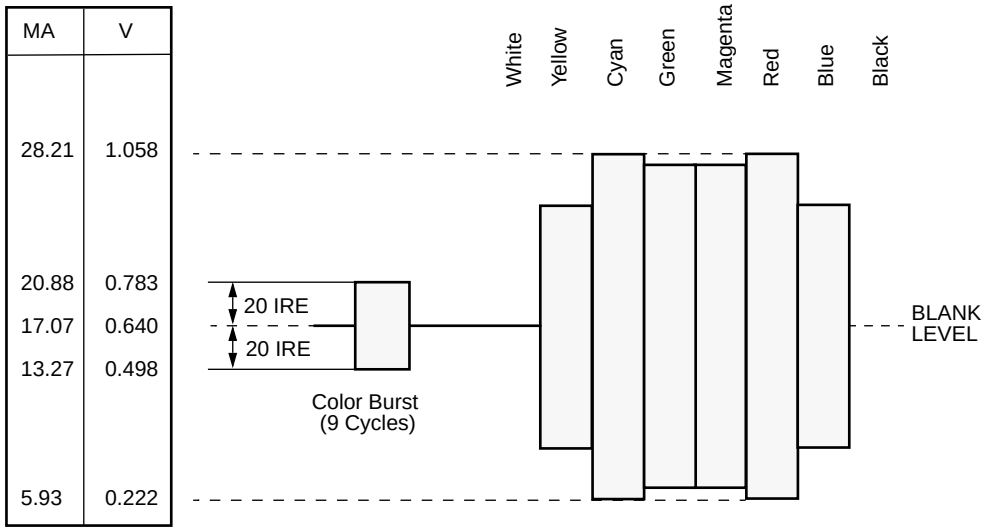
Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, setup off, and nominal RSET. CCIR 624 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.

Table 3. 625-Line (PAL–B, D, G, H, I, N, N-Argentina) Y (Luminance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*
White	26.68	400	0	1
Black	8.00	120	0	1
Blank	8.00	120	0	0
Sync	0	0	1	0

Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, setup off, and nominal RSET. CCIR 624 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.

Figure 11. 525-Line (NTSC/PAL–M) C (Chrominance) Video Output Waveform



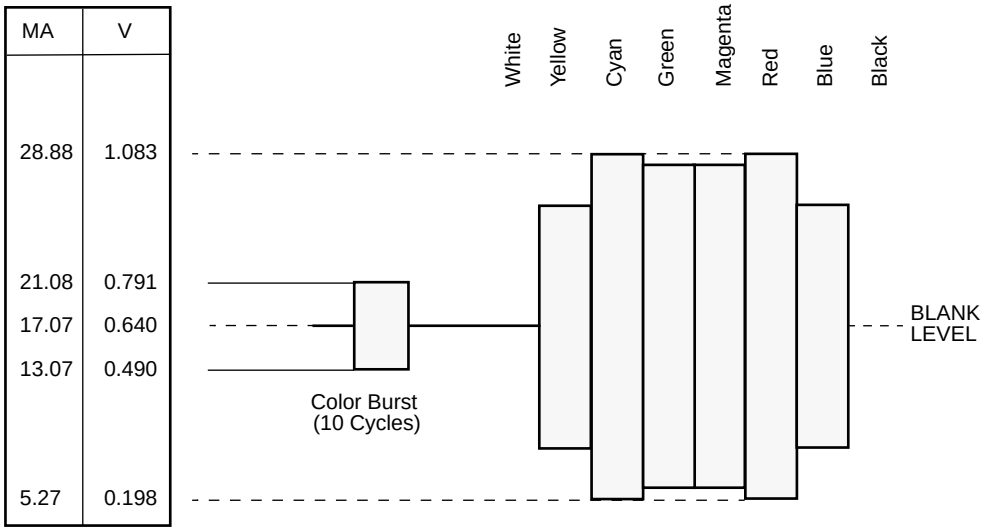
Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, Nominal RSET, Chroma on, and setup on. SMPTE 170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Table 4. 525-Line (NTSC/PAL–M) C (Chrominance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*
Peak Chroma (High)	28.21	423	x	1
Burst (High)	20.88	313	x	x
Blank	17.07	256	x	0
Burst (Low)	13.27	199	x	x
Peak Chroma (Low)	5.93	89	x	1

Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, Nominal RSET, Chroma on, and setup on. SMPTE 170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Figure 12. 625-Line (PAL–B, D, G, H, I, N, N-Argentina) C (Chrominance) Video Output Waveform



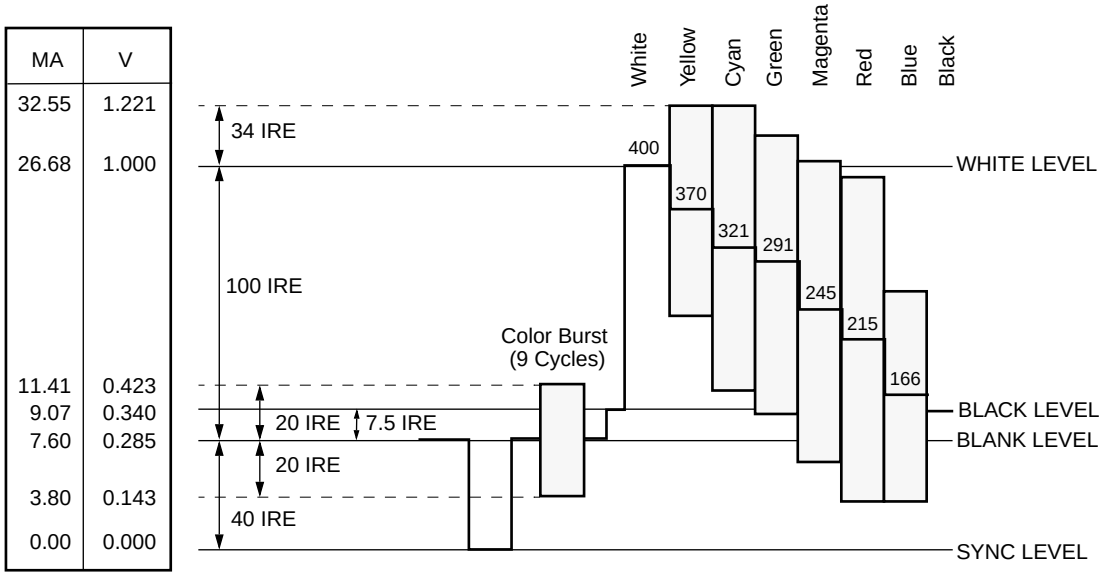
Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, nominal RSET, Chroma on, and setup off. CCIR 624 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.

Table 5. 625-Line (PAL–B, D, G, H, I, N, N-Argentina) C (Chrominance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*
Peak Chroma (High)	28.88	433	x	1
Burst (High)	21.08	316	x	x
Blank	17.07	256	x	0
Burst (Low)	13.07	196	x	x
Peak Chroma (Low)	5.27	79	x	1

Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, nominal RSET. chroma on, and setup off. CCIR 624 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.

Figure 13. Composite 525-Line (NTSC/PAL–M) Video Output Waveform



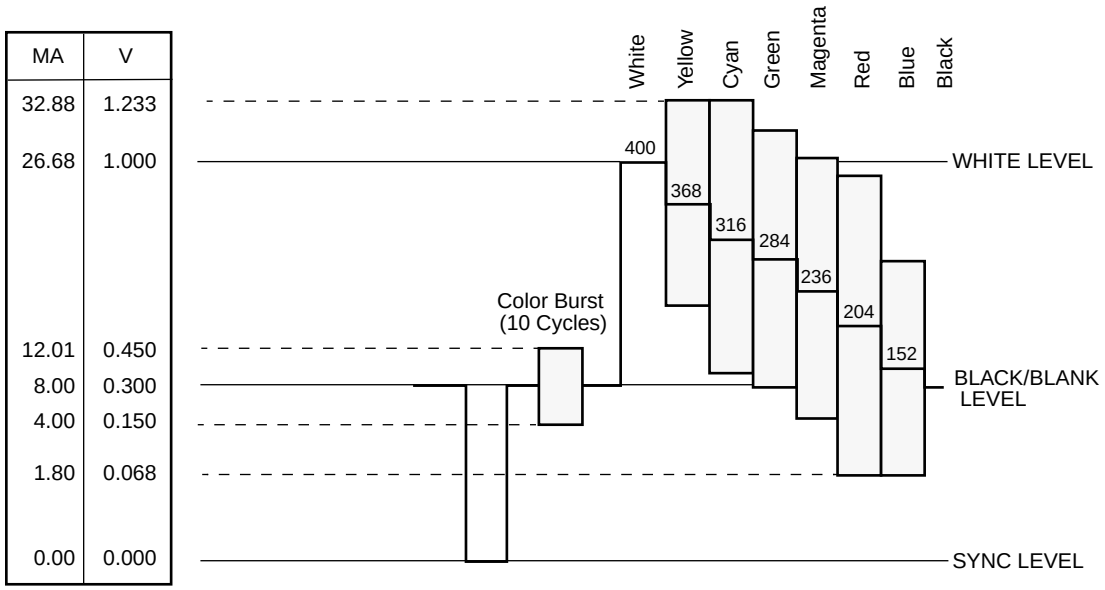
Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, Nominal RSET, clipping off, chroma on and setup on. SMPTE 170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Table 6. Composite 525-Line (NTSC/PAL–M) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*
Peak Chroma (High)	32.55	488	0	1
White	26.68	400	0	1
Burst (High)	11.41	171	0	x
Black	9.07	136	0	1
Blank	7.60	114	0	0
Burst (Low)	3.80	57	0	x
Peak Chroma (Low)	3.20	48	0	1
Sync	0	0	1	0

Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, Nominal RSET, clipping off, chroma on and setup on. SMPTE 170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Figure 14. Composite 625-Line (PAL–B, D, G, H, I, N, N-Argentina) Video Output Waveform



Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, Nominal RSET, setup and clipping off. CCIR 624 levels are assumed. 100% amplitude, 100% saturation (100/0/100/0) color bars are shown.

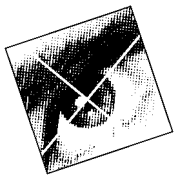
Table 7. Composite 625-Line (PAL–B, D, G, H, I, N, N-Argentina) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*
Peak Chroma (High)	32.88	493	0	1
White	26.68	400	0	1
Burst (High)	12.01	180	0	x
Black	8.00	120	0	1
Blank	8.00	120	0	0
Burst (Low)	4.00	60	0	x
Peak Chroma (Low)	1.80	27	0	1
Sync	0	0	1	0

Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, Nominal RSET, setup and clipping off. CCIR 624 levels are assumed. 100% amplitude, 100% saturation (100/0/100/0) color bars are shown.

Table 8. RGB Output Table (RGBOUT = 1)

Description	Iout (mA)	DAC Data	BLANK*	YC MODE
White	17.04	255	1	0
Black	0	0	1	0
Blank	0	0	0	
White (0xEB)	20.07	301	1	1
Black (0x10)	1.40	21	1	1
Blank	1.40	21	0	1
Note: Iout typical with 37.5 Ω load, VREF_IN = VREF_OUT, nominal RSET.				



REGISTERS

Internal Register

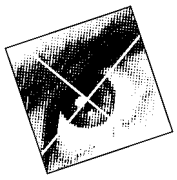
All registers are write-only and set to zero following a reset condition. 7-bit values must be followed by a zero to form the 8-bit address.

I^2C Address = 0x88

Function	Subaddress		Description
	7-bit	8-bit	
Reserved	0x60–0x66, 0x70–0x7F	0xC0–0xCD, 0xE0–0xFF	Reserved. Must be zero for normal operation.
CCDA	0x67	0xCE	First byte of closed-caption data for line 284/335.
CCDB	0x68	0xD0	Second byte of closed-caption data for line 284/335.
CCDC	0x69	0xD2	First byte of closed-caption data for line 21/22.
CCDD	0x6A	0xD4	Second byte of closed-caption data for line 21/22.
HSYNC Begin Time	0x6B	0xD6	This register (non-zero when D7 of registers 0xDA logical one) value specifies the horizontal count (8 least significant bits) when HSYNC* should be asserted. This register is ignored if in slave mode or if bit 7 in register 0xDA is zero. The two most significant bits are in register 0xDA.
HSYNC End Time	0x6C	0xD8	This register (non-zero when D7 of register 0xDA logical one) value specifies the horizontal count (8 least significant bits) when HSYNC* should be deasserted. This register is ignored if in slave mode or if bit 7 in register 0xDA is zero. The two most significant bits are in register 0xDA. A value equal to the begin value is indeterminate.

Function	Subaddress		Description
	7-bit	8-bit	
HSYNC timing	0x6D	0xDA	Bit D7 (ignored in slave mode): 0 = standard HSYNC timing 1 = programmable HSYNC timing Bits D6, D5 (ignored if D7 = 0): Two most significant bits for the HSYNC begin value. Bits D4, D3 (ignored if D7 = 0): Two most significant bits for the HSYNC end value. Bit D2 (active only if bit D4 of register 0xDC = 1): 0 = enable upsampling of RGB outputs 1 = disable upsampling of RGB outputs Bits D1 and D0: 3 = PAL–M 2 = Reserved 1 = PAL–N (Argentina) 0 = PAL–B, D, G, H, I, N
Modes and Control	0x6E	0xDC	Bit D7 (only used when YCMODE pin is high): 0 = 16-bit YCrCb 1 = 8-bit YCrCb Bit D6 (ignored if RGB input format): 0 = Cb0 occurs on odd horizontal count 1 = Cb0 occurs on even horizontal count Bit D5 (affects black level and pixel scaling): 0 = add 7.5 IRE setup for active NTSC/PAL–M lines; do not add setup for active PAL lines 1 = disable 7.5 IRE setup for active NTSC/PAL–M lines; add equivalent 7.5 IRE setup for active PAL lines Bit D4: 0 = use mode pins 1 = override mode pins Bit D3 (active only if D4 = 1): 0 = master mode 1 = slave mode Bit D2 (active only if D4 = 1): 0 = NTSC operation 1 = PAL operation Bit D1 (active only if D4 = 1): 0 = noninterlaced operation 1 = interlaced operation Bit D0 (active only if D4 = 1): 0 = CCIR 601 resolution 1 = square pixel resolution

Function	Subaddress		Description
	7-bit	8-bit	
Caption Mode and Control	0x6F	0xDE	Bit D7 (line 335 for 625-line systems): 0 = disable line 284 extended data services 1 = enable line 284 extended data services Bit D6 (line 22 for 625-line systems): 0 = disable line 21 closed captioning 1 = enable line 21 closed captioning Bit D5: 0 = normal operation 1 = blank chroma portion of video output Bit D4: 0 = normal operation 1 = enable color bars Bit D3 (ignored in master mode): 0 = color subcarrier reset every 4 (NTSC) or 8 (PAL) fields 1 = color subcarrier not locked to field timing Bit D2: 0 = normal operation 1 = blank all lines in vertical blanking interval Bit D1 (DAC level for clipping composite video, ignored if D0=0): 0 = values less than 31 are made 31 1 = values less than 63 are made 63 Bit D0: 0 = disable DAC output clipping 1 = enable DAC output clipping



PC BOARD CONSIDERATIONS

For optimum performance of the Bt856/7, proper CMOS layout techniques should be studied in the Bt451/457/458 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun.

The layout should be optimized for lowest noise on the power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for ground and power, respectively.

Component Placement

Components should be placed as close as possible to the associated pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt856/7 to be located as close as possible to the power supply connector and the video output connector.

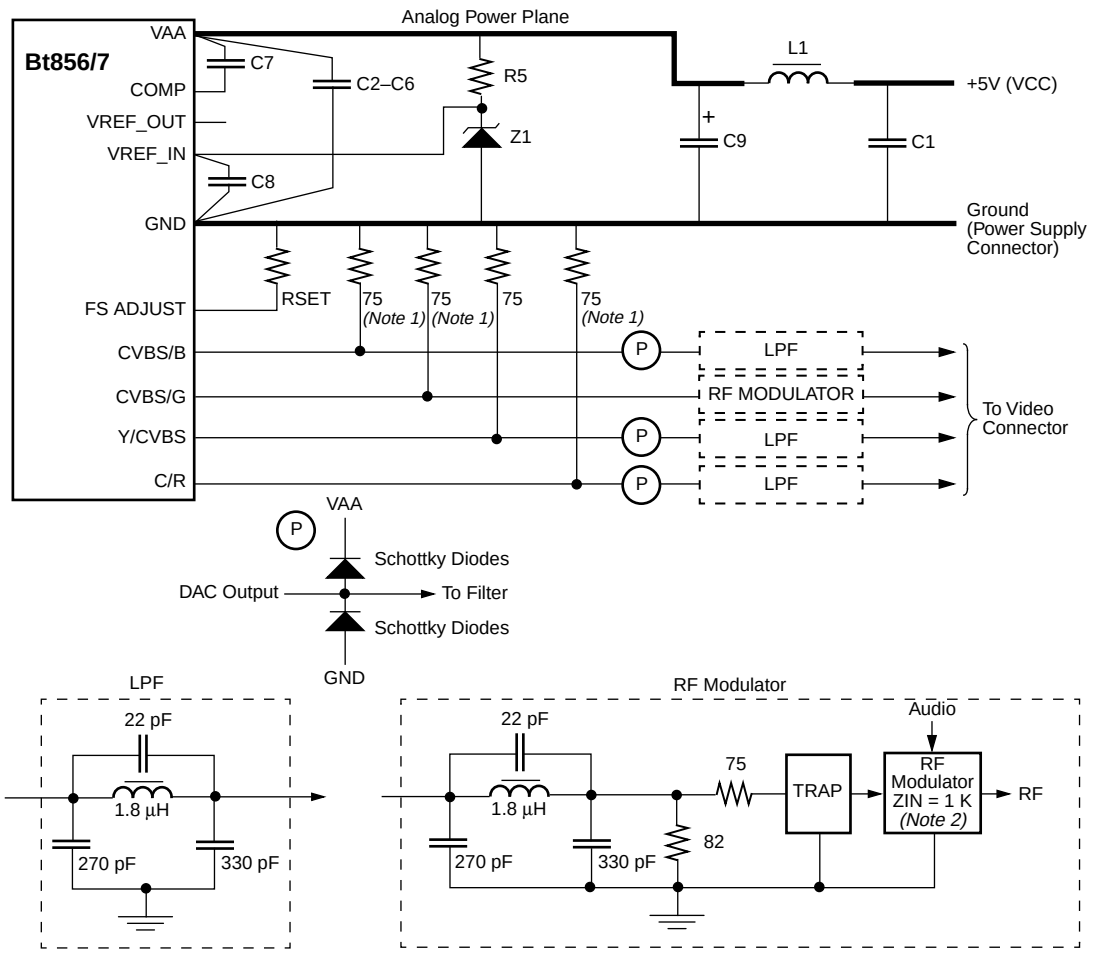
Power and Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt856/7 power pins, VREF_IN circuitry, and COMP decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 15 and 16. This bead should be located within 3 inches of the Bt856/7. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2723021447, or TDK BF45-4001.

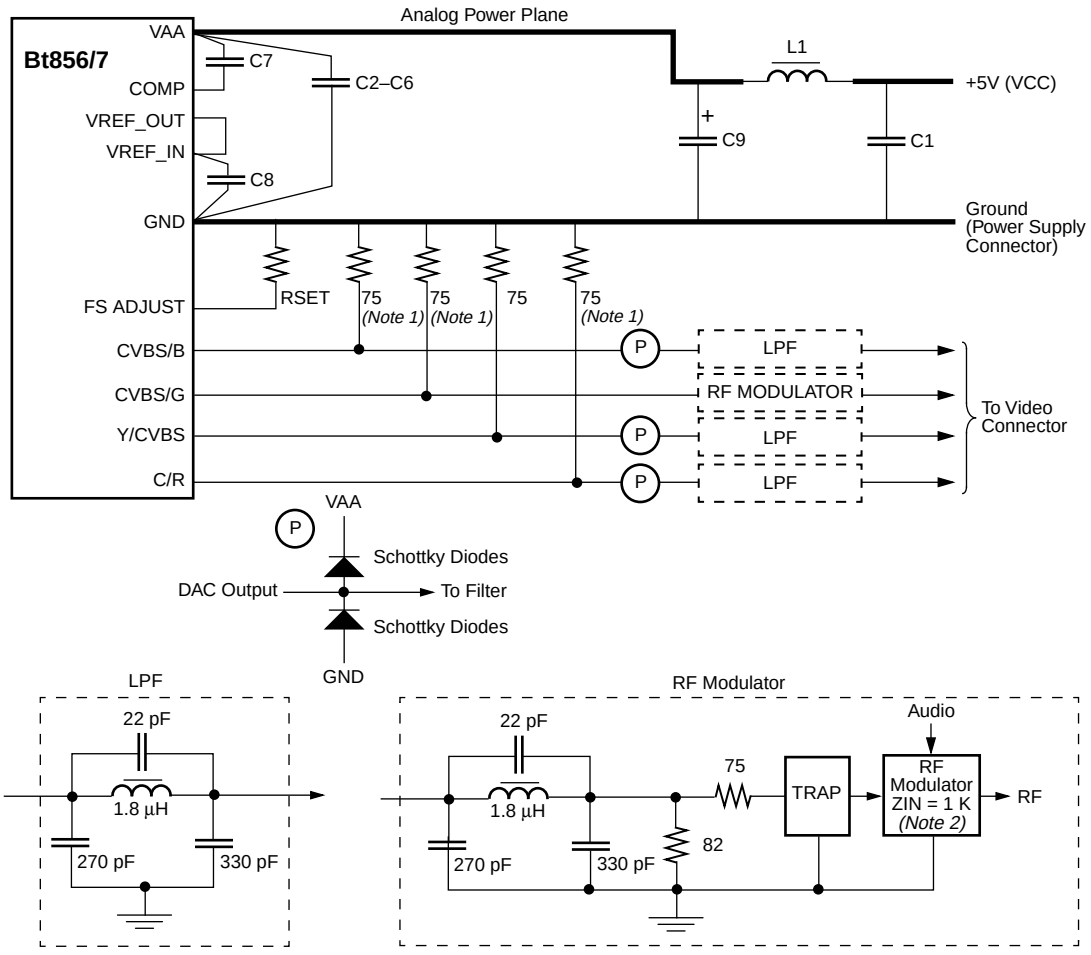
Figure 15. Typical Connection Diagram and Parts List (External Voltage Reference)



Notes: 1. Values for 700 mV SCART/PeriTV may be 20% higher when using RGB inputs.
2. Some modulators may require AC coupling capacitors (10 µF).

Location	Description	Vendor Part Number
C1–C8	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C9	47 µF Capacitor	Mallory CSR13F476KM
L1	Ferrite Bead - Surface Mount	Fair-Rite 2743021447
R1	1 KΩ 5% Resistor	
RSET	1% Metal Film Resistor	Dale CMF-55C
Z1	1.235 V Voltage Reference	LM385BZ–1.2, LM4041-1.2
TRAP	Ceramic Resonator	Murata TPSx.xMJ or MB2 (where x.x =sound carrier frequency in MHz)
	Schottky Diodes	BAT85 (BAT54F Dual) HP 5082-2305 (1N6263) Siemens BAT 64-04 (Dual)
The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt856/7.		

Figure 16. Typical Connection Diagram and Parts List (Internal Voltage Reference)



Notes: 1. Values for 700 mV SCART/PeriTV may be 20% higher when using RGB inputs.
2. Some modulators may require AC coupling capacitors (10 µF).

Location	Description	Vendor Part Number
C1–C8	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C9	47 µF Capacitor	Mallory CSR13F476KM
L1	Ferrite Bead - Surface Mount	Fair-Rite 2743021447
RSET	1% Metal Film Resistor	Dale CMF-55C
TRAP	Ceramic Resonator	Murata TPSx.xMJ or MB2 (where x.x = sound carrier frequency in MHz)
	Schottky Diodes	BAT85 (BAT54F Dual) HP 5082-2305 (1N6263) Siemens BAT 64-04 (Dual)
The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt856/7.		

Decoupling

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply performance is obtained with a 0.1 µF ceramic capacitor decoupling each group of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 47 µF capacitor shown in Figures 15 and 16 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 5% of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA pin 66, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

VREF _IN Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

Signal Interconnect

Digital Signal Interconnect

The digital inputs to the Bt856/7 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one-fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt856/7 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should overlay the ground plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt856/7 to minimize reflections. Unused analog outputs should be connected to GND.

Applications Information

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage. Device damage can produce symptoms of catastrophic failure or erratic device behavior with leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided; they could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA and GND pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage.

Sync and Burst Timing

Table 9 lists the resolutions and clock rates for the various modes of operation.

Table 10 lists the horizontal counter values for the end of horizontal sync, start of color burst, end of color burst, and the first active pixel for the various modes of operation. The front porch is the interval before the next expected falling HSYNC* when outputs are automatically blanked.

The horizontal sync width is measured between the 50% points of the falling and rising edges of horizontal sync.

The start of color burst is measured between the 50% point of the falling edge of horizontal sync and the first 50% point of the color burst amplitude (nominally +20 IRE for NTSC/PAL–M and 150 mV for PAL–B, D, G, H, I, N, N-Argentina above the blanking level).

The end of color burst is measured between the 50% point of the falling edge of horizontal sync and the last 50% point of the color burst envelope (nominally +20 IRE for NTSC/PAL–M and 150 mV for PAL–B, D, G, H, I, N, N-Argentina above the blanking level).

Table 9. Field Resolutions and Clock Rates for Various Modes of Operation

Operating Mode	Active Resolution (pixels)	Total Resolution (pixels)	CLKX1 Frequency (MHz)
NTSC/PAL–M CCIR601 PAL–B, D, G, H, I, N, N–Argentina CCIR601 NTSC Square PIXEL *(Note 1)* PAL–B, D, G, H, I, N, N–Argentina SQUARE PIXEL *(Note 1)*	720 x 240 720 x 288 640 x 240 768 x 288	858 x 262 864 x 312 780 x 262 944 x 312	13.5000 13.5000 12.2727 14.7500
Note 1: PAL–M and PAL–N (Argentina) not available in square pixel format.			

Table 10. Horizontal Counter Values for Various Video Timings

Operating Mode	Front Porch *(Note 1)*		Horizontal Counter Value							
			End of Horizontal Sync		Start of Burst		End of Burst		First Active Pixel	
	Clocks	µs	Clocks	µs	Clocks	µs	Clocks	µs	Clocks	µs
NTSC CCIR601	15	1.11	63	4.66	72	5.33	105	7.77	123	9.10
PAL–B, D, G, H, I, N CCIR601	11	0.81	63	4.66	76	5.62	106	7.84	133	9.84
NTSC Square Pixel	18	1.47	58	4.73	65	5.30	96	7.82	117	9.53
PAL–B, D, G, H, I, N Square Pixel	23	1.42	69	4.68	83	5.63	116	7.86	155	10.51
PAL–M CCIR601 *(Note 1, Table 9)*										
PAL–N (Argentina)	15	1.11	63	4.66	78	5.78	111	8.22	123	9.10
CCIR601*(Note 1, Table 9)*	11	0.81	63	4.66	76	5.62	111	8.22	133	9.84

Notes: 1. In slave mode, since Front Porch timing is triggered by the previous HSYNC pulse, any deviation from nominal line length will affect the front porch duration.
2. Timings may differ from Broadcast (e.g. FCC) or Distribution (e.g. RS170) standards, in part due to definitions. BLANK* may be asserted to prolong porch intervals. Chroma blanking is effective 10 CLOCK cycles later.

Clock and Subcarrier Stability

The color subcarrier is derived directly from the CLKX2 input, hence any jitter or frequency deviation of CLKX2 will be transferred directly to the color subcarrier. Jitter within the valid CLKX2 cycle interval (i.e., for correct registering of CLKX1 and data) will result in hue noise on the color subcarrier on the order of 0.9–1.6 degrees per nanosecond. Random hue noise can result in degradation in AM/PM noise ratio (typically around 40 dB for consumer media such as Videodiscs and VCRs). Periodic or coherent hue noise can result in differential phase error (which is limited to 10 degrees by FCC cable TV standards). Any frequency deviation of the CLOCK from nominal will challenge the subcarrier tracking capability of the destination receiver. This may range from a few parts-per-million (ppm) for broadcast equipment to 100 ppm for industrial equipment to a few hundred ppm for consumer equipment. Greater subcarrier tracking range generally results in poorer subcarrier decoding dynamic range, so that receivers that tolerate jitter and wide subcarrier frequency deviation will introduce more noise in the decoded image. Crystal-based clock sources with maximum deviations of 100 ppm produce the best results for consumer and industrial applications, while temperature-compensated clock sources with tighter tolerances may be warranted for broadcast or more stringent PAL (e.g., type I) applications.

Some applications call for maintaining correct Subcarrier-Horizontal phasing (SC-H) for correct color framing, which requires subcarrier coherence within specified tolerances over a four-field interval for 525-line systems or 8 fields for 625-line systems. Any CLKX2 interruption (even during vertical blanking interval) which results in mis-registration of the CLKX1 input or non-standard pixel counts per line can result in SC-H excursions outside the NTSC limit of ±40 degrees (reference EIA RS170A) or the PAL limit of ±20 degrees (reference EBU D23-1984).

Any deviation of the number CLKX1 cycles between HSYNC* falling edges when in SLAVE mode may result in automatic mode switching unless the internal control registers at 8-bit subaddress 0xDC are set for the desired mode of operation.

Filtering RF Modulator Connection

The Bt856/7 internal upsampling filter alleviates external filtering requirements by moving significant sampling alias components above 19 MHz and reducing the sinx/x aperture loss up to the filters passband cutoff of 5.75 MHz. While typical chrominance subcarrier decoders can handle the Bt856/7 output signals without analog filtering, the higher frequency alias products pose some EMI concerns and may create troublesome images when introduced to an RF modulator. When the video is presented to an RF modulator, it should be free of energy in the region of the aural subcarrier (4.5 MHz for NTSC, 5.5–6.5 MHz for PAL), hence some additional frequency traps may be necessary when the video signal contains fundamental or harmonic energy (as from unfiltered character generators) in that region. Where better frequency response flatness is required, some peaking in the analog filter is appropriate to compensate for residual digital filter losses with sufficient margin to tolerate 10% reactive components.

A three-pole elliptic filter (1 inductor, 3 capacitors) with a 6.75 MHz passband can provide at least 45 dB attenuation (including sinx/x loss) of frequency components above 20 MHz and provide some flexibility for mild peaking or special traps. An inductor value with a self-resonant frequency above 80 MHz is chosen so that its intrinsic capacitance contributes less than 10% of the total effective circuit value. The inductor itself may induce 1% (0.1 dB) loss. Any additional ferrites introduced for EMI control should have less than 5 Ω impedance below 5 MHz to minimize additional losses. The capacitor to ground at the Bt856/7 output pin is compensated for the parasitic capacitance of the chip plus any protection diodes and lumped circuit traces (about 22 pF+5 pF/diode). Some filter peaking can be accomplished by splitting the 75 Ω source impedance across the reactive PI filter network. However, this will also introduce some chrominance-luminance delay distortion in the range of 10–20 ns for a maximum of 0.5 dB boost at the subcarrier frequency.

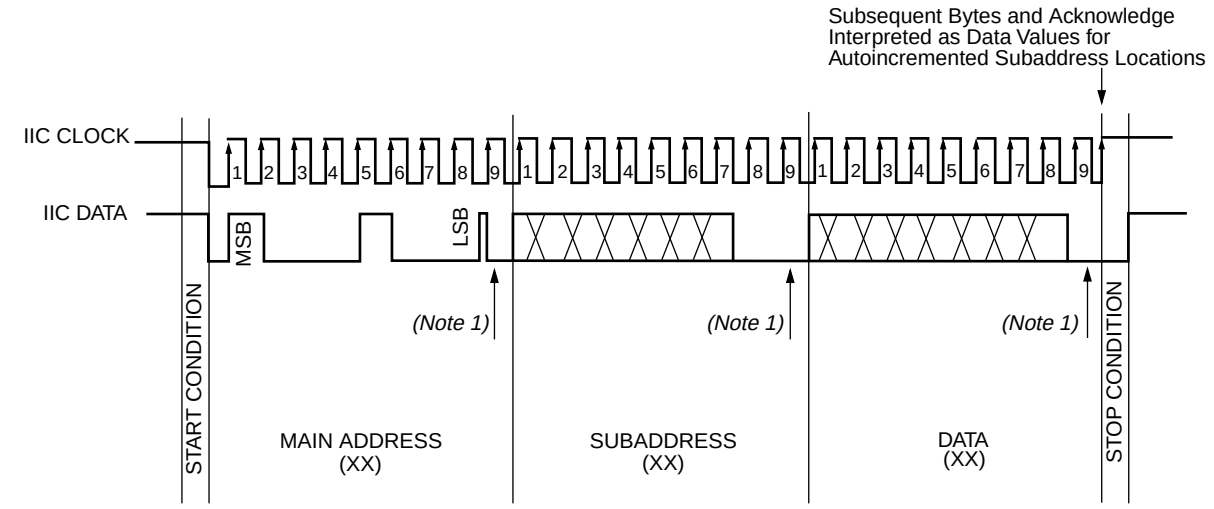
The filter network feeding an RF modulator may include the aforementioned trap, which could take two forms depending on the depth of attenuation and type of resonator device employed. The RF modulator typically has a high input impedance (about 1K ± 30%) and loose tolerance. Consequently, the amplitude variation at the modulator input will be greater, especially when the trap is properly terminated at the modulator input for maximum effect. Some modulators video or aural fidelity will degrade dramatically when overdriven, so the value of the effective termination (nominally 37.5 Ω) may need to be adjusted downward to maintain sufficient linearity (or depth of modulation margin) in the RF signal. When using a two section strap (e.g., when stereo, SAP, or AM aural carriers are generated), some impedance isolation (e.g., buffer) may be required before the trap to obtain flattest frequency response. See Figures 15 and 16.

I²C Programming

Data Transfer on the I²C Bus

Figure 17 shows the relationship between IIC DATA and IIC CLOCK to be used when programming the I²C bus. If the bus is not being used, both IIC DATA and IIC CLOCK lines must be left high.

Figure 17. IIC Diagram



Note 1: Acknowledge generated by Bt856/7.

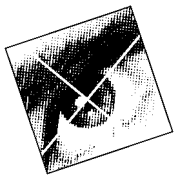
Every byte put onto the IIC DATA line should be 8 bits long (MSB first), followed by an acknowledge bit, which is generated by the receiving device.

Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always the address byte. If this is the device's own address, the device will generate an acknowledge by pulling the IIC DATA line low during the ninth clock pulse, then accept the data in subsequent bytes (autoincrementing the subaddress) until another stop condition is detected.

The eighth bit of the address byte is the read/write bit (high = read from addressed device, low = write to the addressed device) so, for the Bt856/7, the address is only considered valid if the R/W bit is low.

Data bytes are always acknowledged during the ninth clock pulse by the addressed device. Note that during the acknowledge period the transmitting device must leave the IIC DATA line high.

Premature termination of the data transfer is allowed by generating a stop condition at any time. When this happens, the Bt856/7 will remain in the state defined by the last complete data byte transmitted. Any master acknowledge subsequent to reading the chip ID (subaddress 0x89) is ignored.



PARAMETRIC INFORMATION

DC Electrical Parameters

Table 11. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		70	°C
DAC Output Load *(Note 1)*	RL		37.5		Ω
Nominal RSET using internal VREF using external VREF (1.23 V)	RSET		 71.5 73.2		 Ω Ω
External VREF	VREF	1.15	1.235	1.32	V
Note 1: DC component not to exceed 80 Ω.					

Table 12. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin *(Note 1)*		GND –0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		Indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 Minute)	TVSOL			220	°C

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply or ground voltage by more than 0.5 V can cause destructive latchup.

DC Characteristics

Table 13. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Video D/A Resolution		9	9	9	Bits
Output Current-DAC Code 511 (Iout FS)			34.08	40	mA
Output Voltage-DAC Code 511			1.28		V
Video Level Error					
Using External Reference (RSET Trim, Nominal Load)				5	%
Using Internal Reference (Nominal Resistors				5	%
Output Capacitance			22		pF
Digital Inputs (Except those specified below)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND –0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
IIC CLOCK, IIC DATA	VIL	GND –0.5		1.0	V
SLEEP Input					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND –0.5		0.6	V
CLKX2 Input					
Input High Voltage	VIH	2.4		VAA + 0.5	V
Input Low Voltage	VIL	GND –0.5		0.8	V
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
Three-State Current	IOZ			50	µA
Output Capacitance	CDOUT		10		pF
VREF_IN Input Current	IREF_IN		10		µA

"Recommended Operating Conditions," NTSC CCIR 601 operation, and CLKX1 frequency = 13.5 MHz. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

Table 14. AC Characteristics *(1 of 2)*

Parameter	EIA/TIA 250C Ref	Symbol	Min	Typ	Max	Units
Hue Accuracy *(Note 1, Note 3)*				1.5	2.5	± °
Color Saturation Accuracy *(Note 1, Note 3)*				1.5	2.0	± %
Chroma AM/PM Noise *(Note 3)*	1 MHz Red Field			–62		dB rms
Differential Gain *(Note 2)*	6.2.2.1			1.5		% p–p
Differential Phase *(Note 2)*	6.2.2.2			1.0		° p–p
SNR (unweighted 100 IRE Y Ramp Tilt Correct) *(Note 2)*						
RMS	6.3.1			60		dB rms
Peak Periodic	6.3.2		55	56		dB p-p
100 IRE Multiburst *(Note 3)*	6.1.1			–2.2	6	± IRE
Chroma/Luma Gain Ineq *(Note 3)*	6.1.2.2			–5	3	± IRE
Chroma/Luma Delay Ineq *(Note 3)*	6.1.2		–6	4		ns
Short Time Distortion 100IRE/PIXEL *(Note 3)*	6.1.6			0		%
Luminance Nonlinearity *(Note 2)*	6.2.1			2	1.0	%
Chroma/Luma Intermod *(Note 2)*	6.2.3			0.1	1.0	± IRE
Chroma Nonlinear Gain *(Note 2)*	6.2.4.1		–1.0			± IRE
Chroma Nonlinear Phase *(Note 2)*	6.2.4.2		–1.0			± °
Pixel/Control Setup Time *(Note 4)*		1	7			ns
Pixel/Control Hold Time *(Note 4)*		2	3			ns
YCMODE/GAMMA* Setup Time *(Note 5)*		1	6			ns
YCMODE/GAMMA* Hold Time *(Note 5)*		2	4			ns
Control Output Delay Time *(Note 4)*		3			17	ns
Control Output Hold Time *(Note 4)*		4	2			ns
CLOCK Frequency (I/T)		Fin	12.27		14.75	MHz
CLKX1 Setup Time		5	8			ns
CLKX1 Hold Time		6	0			ns
CLKX2 Frequency			24.54		29.50	MHz
CLKX2 Pulse Width Low Time			8			ns
CLKX2 Pulse Width High Time			8			ns

"Recommended Operating Conditions," NTSC CCIR 601 operation, and CLKX1 frequency = 13.5 MHz. Analog output load ≤ 75 pF. HSYNC*, VSYNC*, BLANK*, and FIELD output load ≤ 75 pF. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V. Video input and output timing is shown in Figures 18 and 19.

Notes: 1. 75/7.5/75/7.5 Color bars normalized to burst.
2. Guaranteed by characterization.
3. Without post filter. Guaranteed by design.
4. Control pins are defined as: R0–R7, G0–G7, B0–B7, BLANK*, HSYNC*, VSYNC*, FIELD, YCMODE, GAMMA*.
5. For YCMODE and GAMMA* inputs in 8-bit YC mode ONLY

Table 14. AC Characteristics *(2 of 2)*

Parameter	EIA/TIA 250C Ref	Symbol	Min	Typ	Max	Units
Pipeline Delay Input Pixels to Composite Video Input Pixels to RGB Output			 25.5 10.5	 25.5 10.5	 25.5 10.5	 T T
VAA Supply Current				250	295	mA
Power-Down Mode Current					15	mA
"Recommended Operating Conditions," NTSC CCIR 601 operation, and CLKX1 frequency = 13.5 MHz. Analog output load ≤ 75 pF. HSYNC*, VSYNC*, BLANK*, and FIELD output load ≤ 75 pF. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V. Video input and output timing is shown in Figures 18 and 19.						

Figure 18. 24-bit RGB and 16-bit YCrCb Video Input and Output Timing

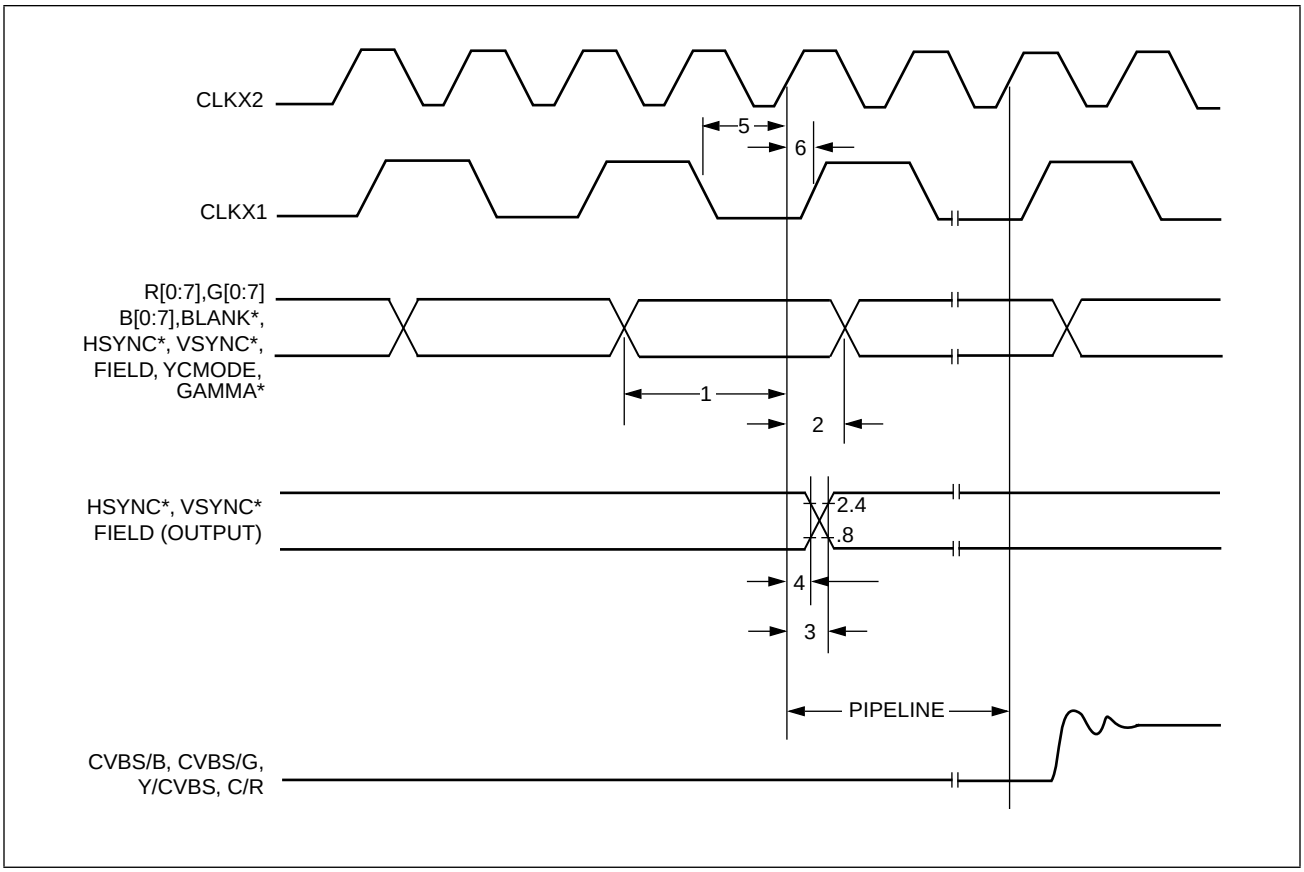
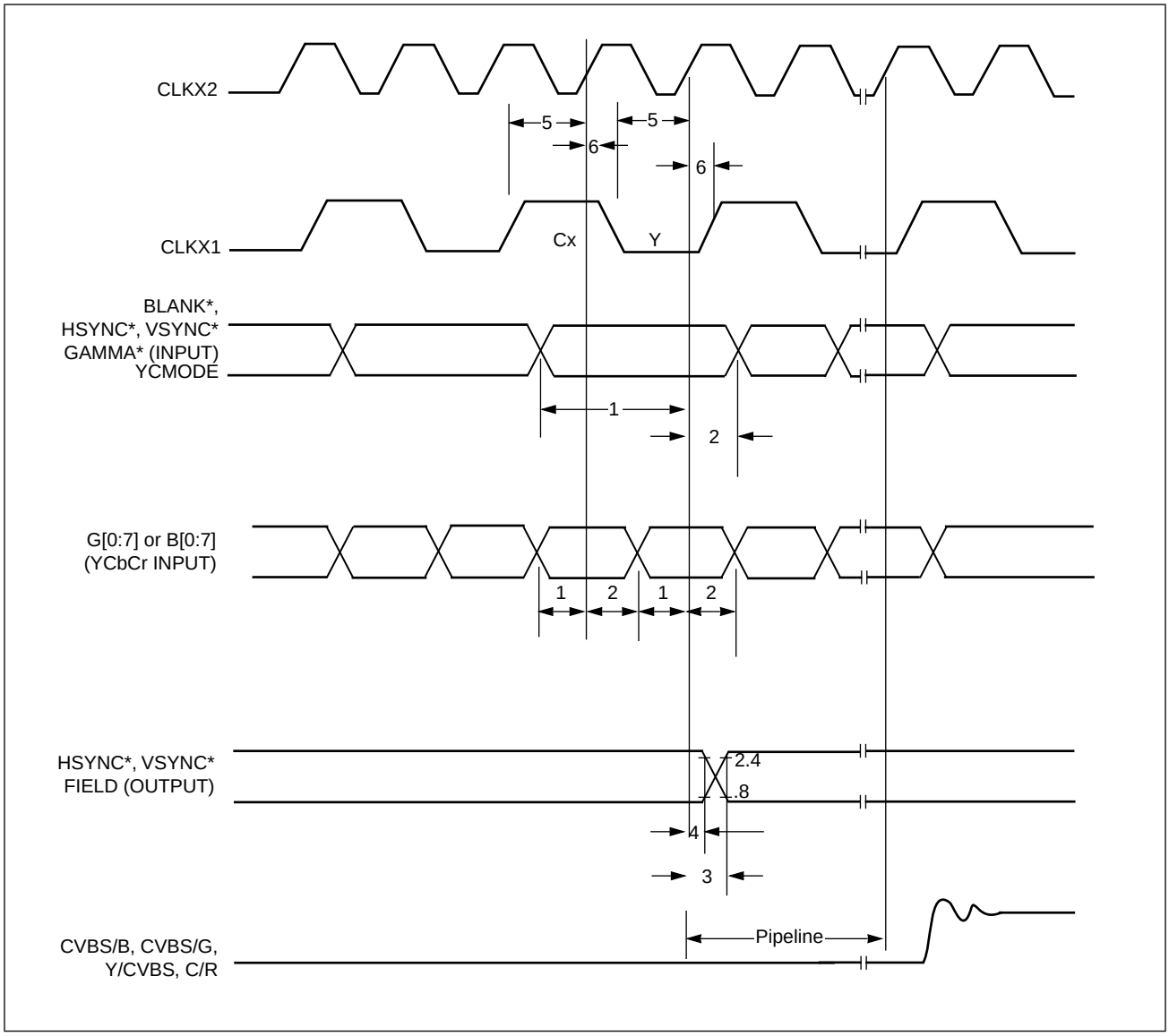
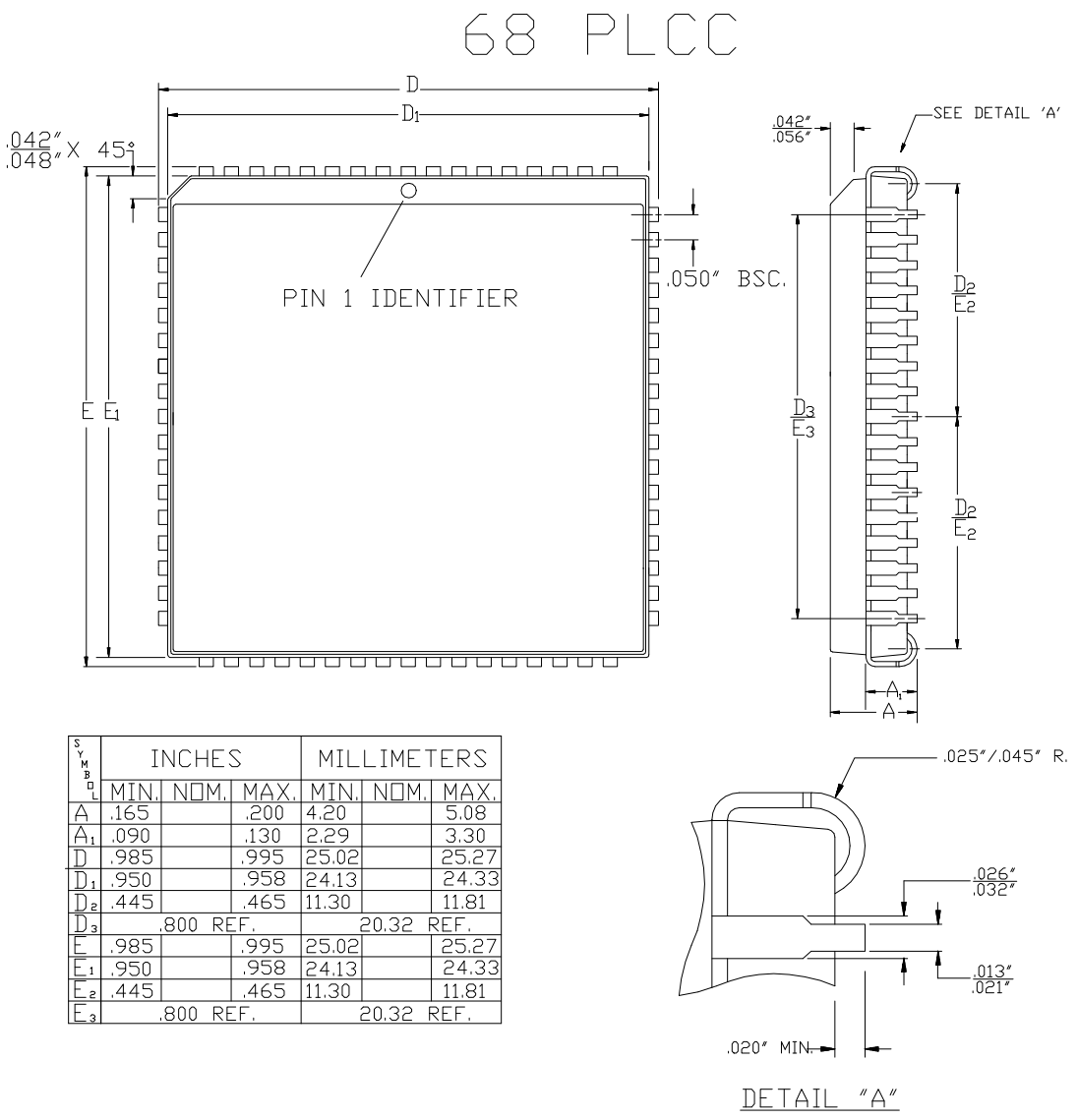


Figure 19. 8-bit YCrCb Video Input and Output Timing



Package Drawing

Figure 20. 68-Pin PLCC



SYMBOL	INCHES			MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	.165		.200	4.20		5.08
A_1	.090		.130	2.29		3.30
D	.985		.995	25.02		25.27
D_1	.950		.958	24.13		24.33
D_2	.445		.465	11.30		11.81
D_3	.800 REF.			20.32 REF.		
E	.985		.995	25.02		25.27
E_1	.950		.958	24.13		24.33
E_2	.445		.465	11.30		11.81
E_3	.800 REF.			20.32 REF.		

Revision History

Revision	Change from Previous Revision
A	Initial Release
B	Revised Pin Assignments for RGB Outputs
C	Added PAL–M, PAL–N (Argentina), Final AC/DC Specifications

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